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NEC:LunarEagle

MSI:MS-7420N1

Version:0C



CPU: Conroe family processors /WolfDale/Yorkfield in LGA775 Package.

System Chipset:

Intel EagleLake-Q+Intel ICH10-DO

On Board Device:

BIOS -- SPI Flash 32M

LAN --INTEL 82567LM Boazman

Super I/O -- SMSC5617C

AUDIO -- Realtek HD ALC262VD

Clock GEN-IDTCV184-2

TPM-SLB 9635 TT1.2

Main Memory:

Due-channel DDR-III * 2 (1066MHZ)

Intersil PWM:


Controller: Intersil ISL6334 (3 Phases)

Expansion Slots:

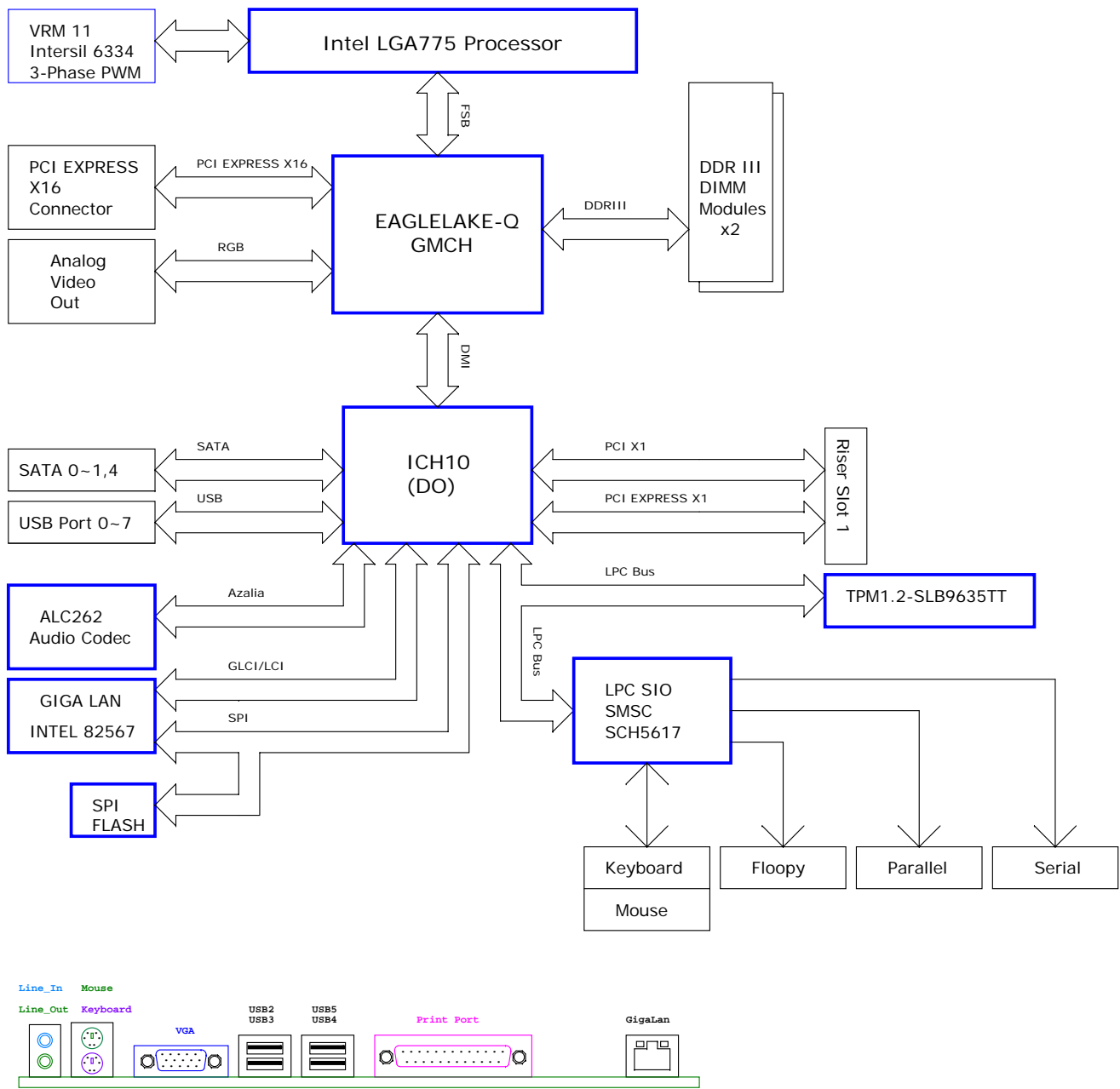
PCI-E(X16) Slot *1

Riser Slot :(PCIx1/PCI-E(x1)x1)

MS-6497N1	ERP Number	Function
MS-7420-0C	601-7420-C10	Mainboard
MS-4046-2A	604-4046-020	Power Button/LED board
MS-4085-10	604-4085-030	Front Audio Board
MS-4048-41	604-4048-050	Front USB Board
MS-4121-10	604-4121-010	Riser Card

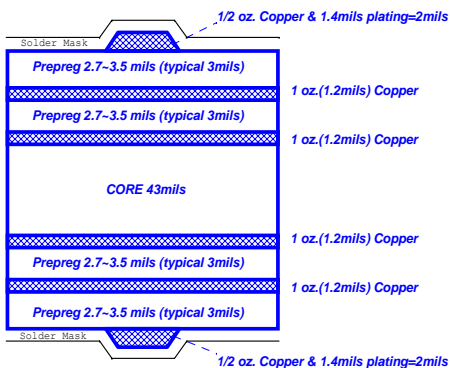
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Title COVER SHEET		
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Block Diagram



Board Stack-up (6 layers)

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
IEEE1394 - 110ohm : 15/4/9/4/15
Differential Clock : 18/4/10/4/18

Example Fab Drawing Note (1080 Prepreg PCB)


Trace Width (mils)	Differential Spacing (mils)	Target Impedance	Tolerance
4.0	NA	50-ohm, single-ended	15%
6.5	NA	40-ohm, single-ended	15%
7.5	NA	30-ohm, single-ended	15%
9.5	NA	32-ohm, single-ended	15%
3.9	8.1	95-ohm, differential	20%, reference only
4.5	7.5	90-ohm, differential	20%, reference only

Eaglelake(GMCH) Impedance Requirements by Interface

Interface	Impedance Required
FSB (All)	4x signals 42-ohm, others 50-ohm, single-ended
Controller Link	50-ohm, single-ended
DDR2 (DQ, DQS, DM, CLK, CLK#)	40-ohm, single-ended
DDR2 (Control)	43-ohm, single-ended
DDR2 (Command)	33-ohm, single-ended
DDR3 (CLK, CLK#)	36-ohm, single-ended
DDR3 (DQ, DQS, DM)	20/37-ohm, single-ended
DDR3 (Control)	36-ohm, single-ended
DDR3 (Command)	32-ohm, single-ended
PCI Express, DMI	95-ohm, differential
VGA	97-ohm, single-ended at MCH breakout, then 50-ohm, single-ended to VGA connector

ICH10 Impedance Requirements by Interface

Interface	Impedance Required
PCI	50-ohm, single-ended
Controller Link	50-ohm, single-ended
Miscellaneous	50-ohm, single-ended
PCI Express, DMI	95-ohm, differential
SATA	95-ohm, differential
USB	90-ohm, differential

 MICRO-START INTL CO., LTD.		
Title BLOCK DIAGRAM		
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CPU SIGNAL BLOCK

7 H_A# [3..35]

7 H_DB# [0..3]

4 H_IERR#

4,15 H_FERR#

15 H_STPCLK#

15 H_INIT#

7 H_DBSY#

7 H_DRDY#

7 H_TRDY#

7 H_ADS#

7 H_LOCK#

7 H_BNR#

7 H_HIT#

7 H_HITM#

7 H_BPR#

7 H_DEFER#

4,15 TRMTRIP#

4,21,28 H_PROCHOT#

15 H_IGNNE#

15 ICH_H_SM#

15 H_A20M#

8,21 H_SLP#

VTT_OUT_LEFT

VTT_OUT_RIGHT

4,6,8 H_FSBSEL0

4,6,8 H_FSBSEL1

4,6,8 H_FSBSEL2

4,15 H_PWRGD

4,7,8,21 H_CPURST#

7 H_D# [0..63]

U20A

DBR#

VCC_SENSE

VSS_SENSE

VCC_MB_REGULATION

VSS_MB_REGULATION

ITP_CLK1

ITP_CLK0

VID_SELECT

GTREF0

GTREF1

GTREF_SEL

CS_GTREF

BPM5#

BPM4#

BPM3#

BPM2#

BPM1#

BPM0#

PCREQ#

REQ4#

REQ3#

REQ2#

REQ1#

REQ0#

TESTH12

TESTH11

TESTH10

TESTH9

TESTH8

TESTH7

TESTH6

TESTH5

TESTH4

TESTH3

TESTH2

TESTH1

TESTH0

FORCEPH

RSVD

BLCK1#

BLCK0#

RS2#

RS1#

RS0#

AP1#

AP0#

BR0#

COMP5

COMP4

COMP3

COMP2

COMP1

COMP0

DP3#

DP2#

DP1#

DP0#

ADSTB1#

ADSTB0#

DSTBP3#

DSTBP2#

DSTBP1#

DSTBP0#

DSTBN3#

DSTBN2#

DSTBN1#

DSTBN0#

LINT1/NMI

LINT0/INTR

ZIF-SOCK775-15u-in

RN23 8P4R-51R0402

RN21 8P4R-680R-LF

RN26 8P4R-680R-LF

PLACE BPM TERMINATION NEAR CPU

BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	267 MHZ (1067)
0 1 0	200 MHZ (800)
0 0 1	133 MHZ (533)
1 0 0	333 MHZ (1333)

MSI
Link to the Future
MICRO-START INTL CO., LTD.

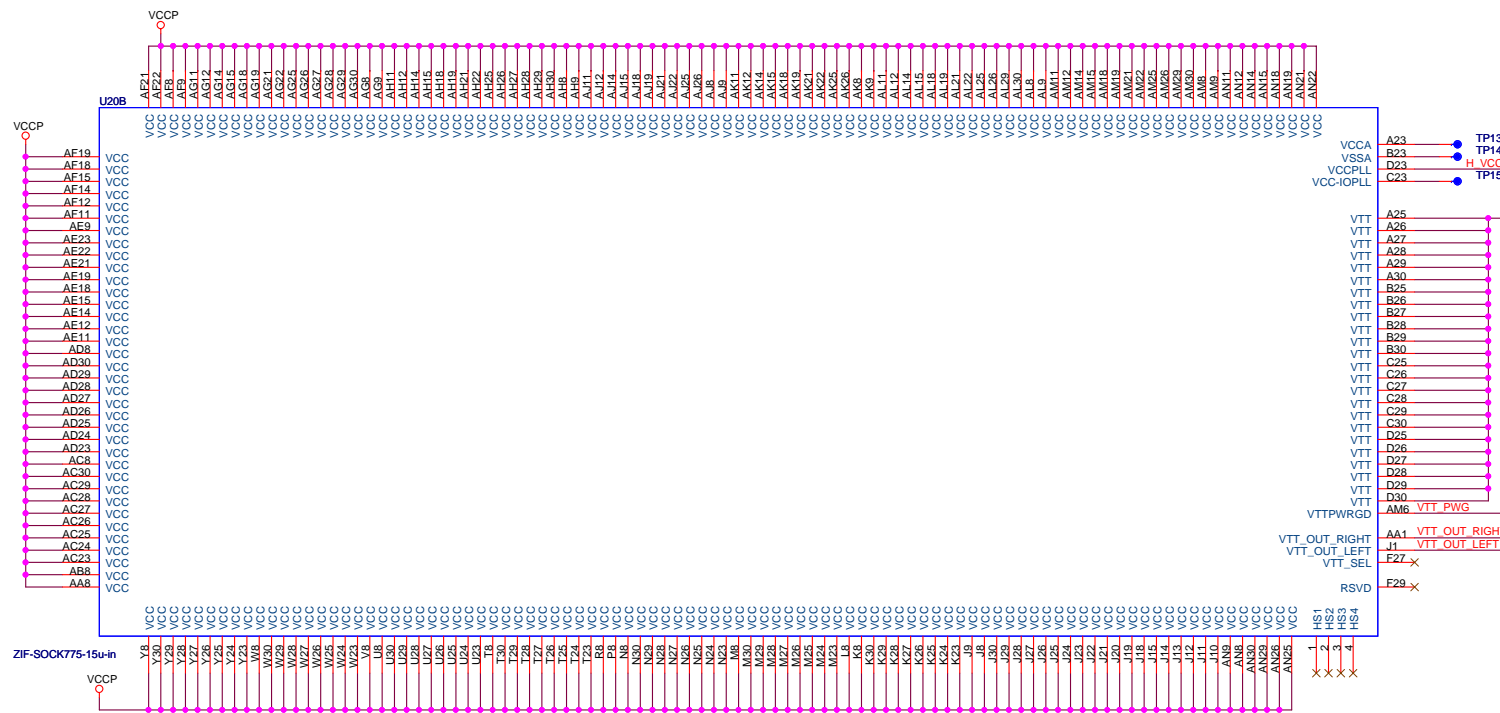
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INTEL LGA775 CPU SIGNAL

Size
Document Number
MS-7420N1

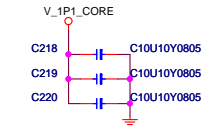
Rev
OC

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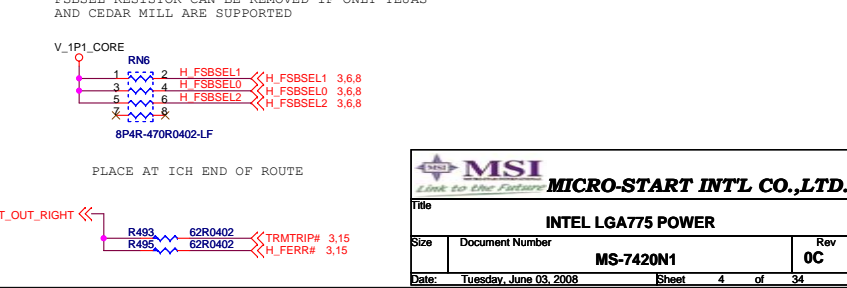
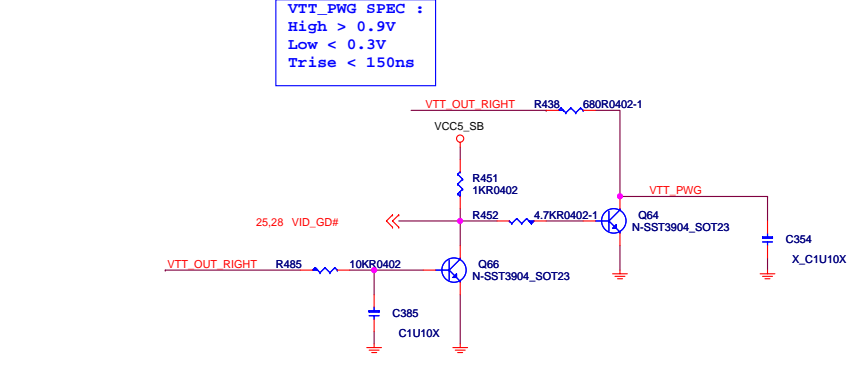
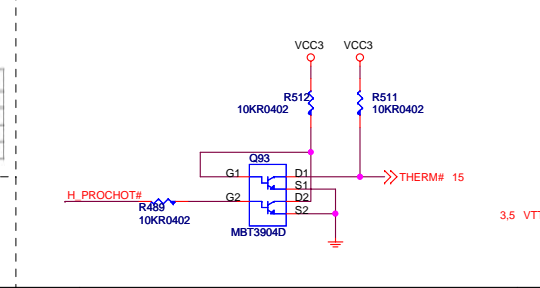
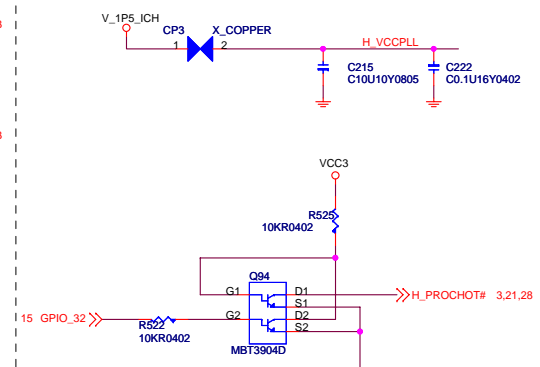
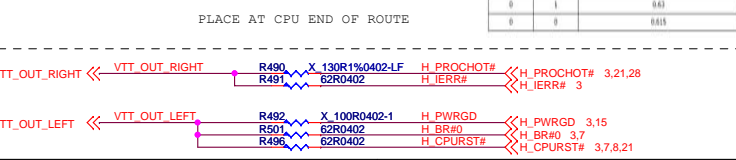
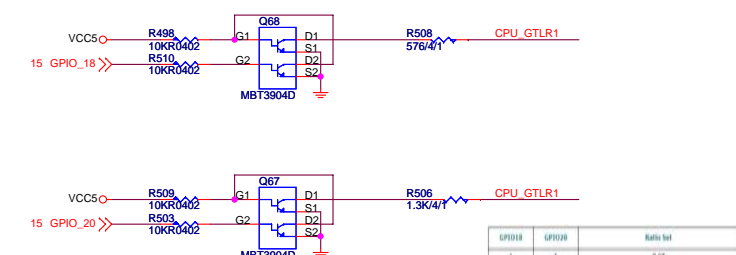
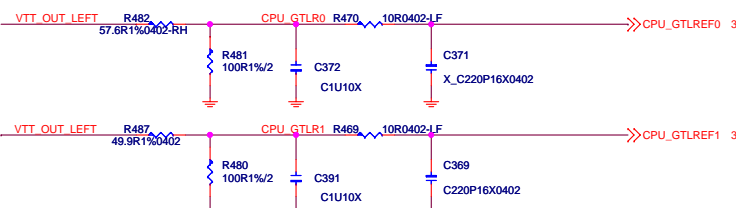
BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)
1	0	0	333 MHZ (1333)



BIOS writers Guide
PDG:page109



CAPS FOR FSB GENERIC



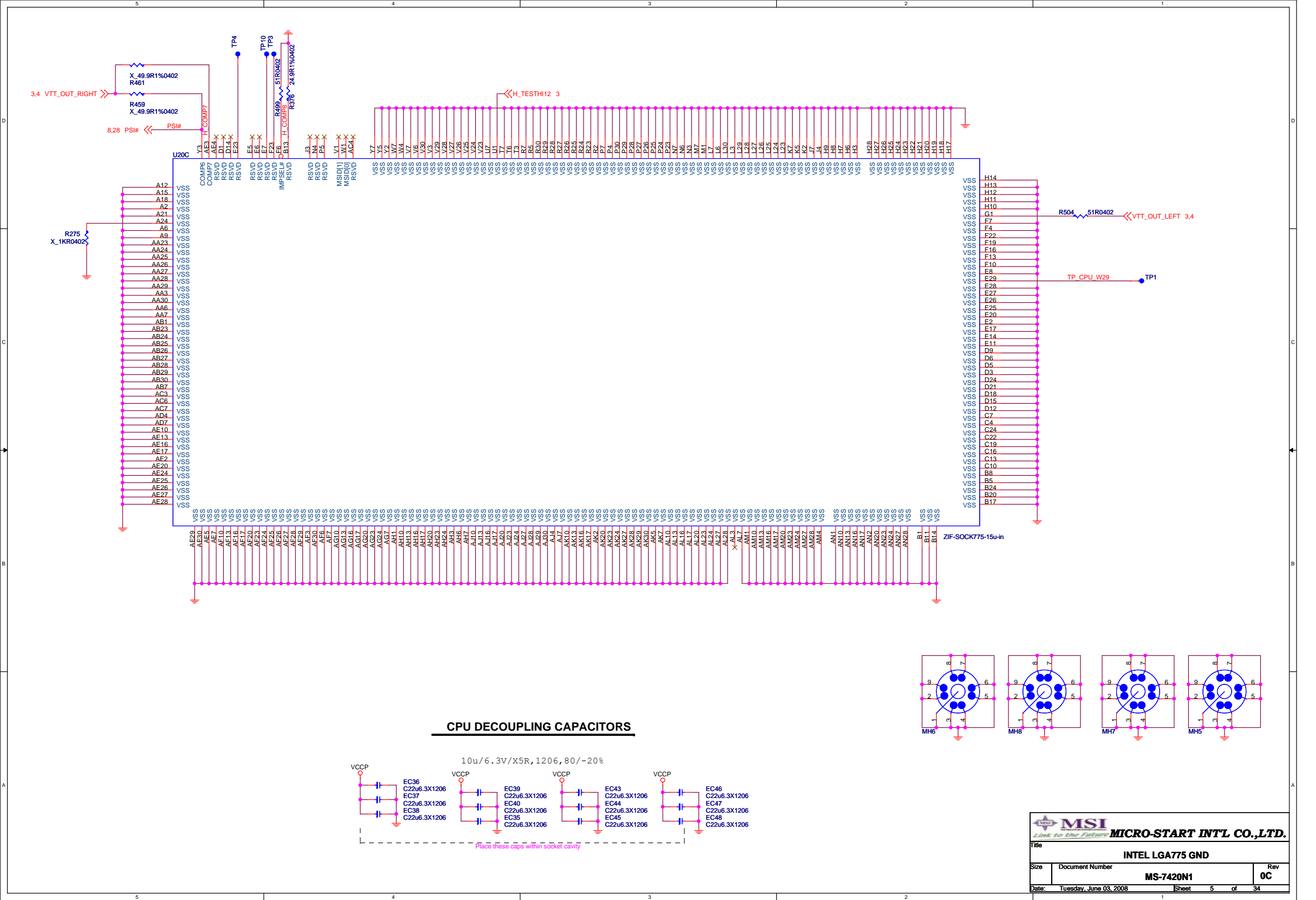
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS
AND CEDAR MILL ARE SUPPORTED

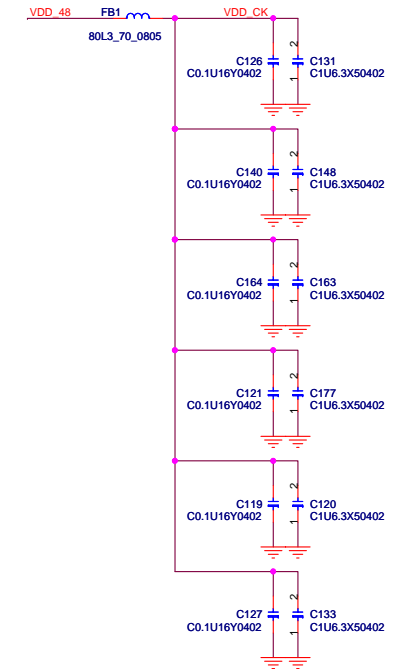
PLACE AT ICH END OF ROUTE

PLACE AT CPU END OF ROUTE

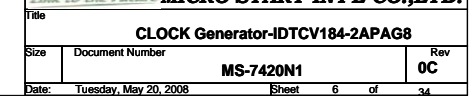
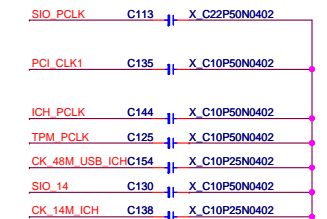
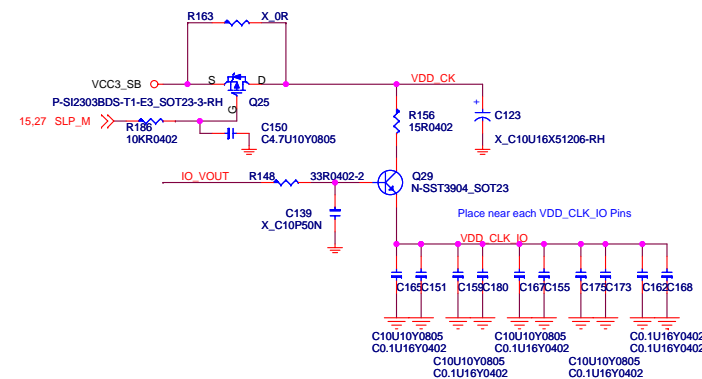
CPURST#	CPURST#	Ratio Test
1	1	0.67
1	0	0.65
0	1	0.63
0	0	0.61

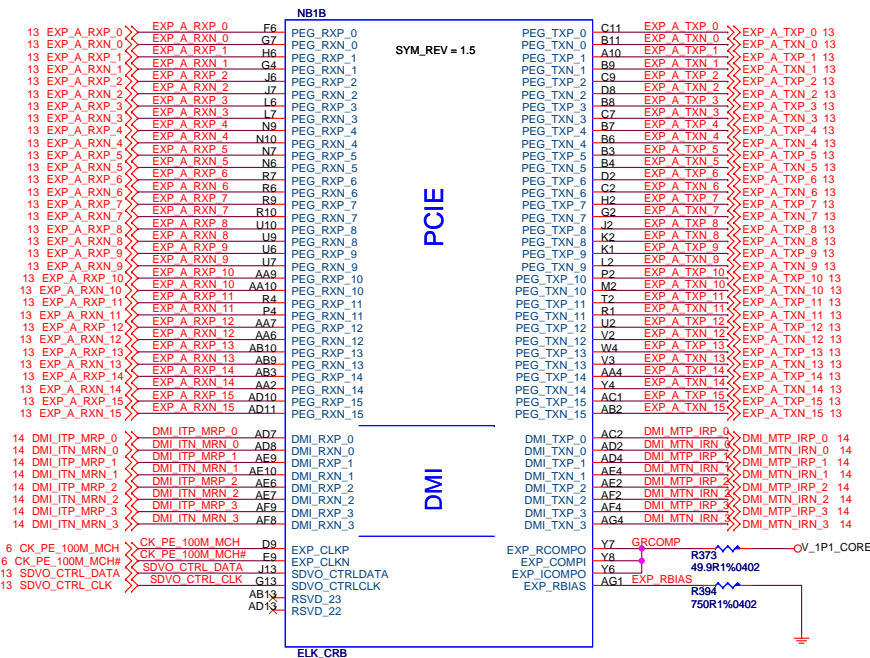


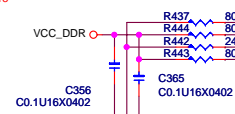
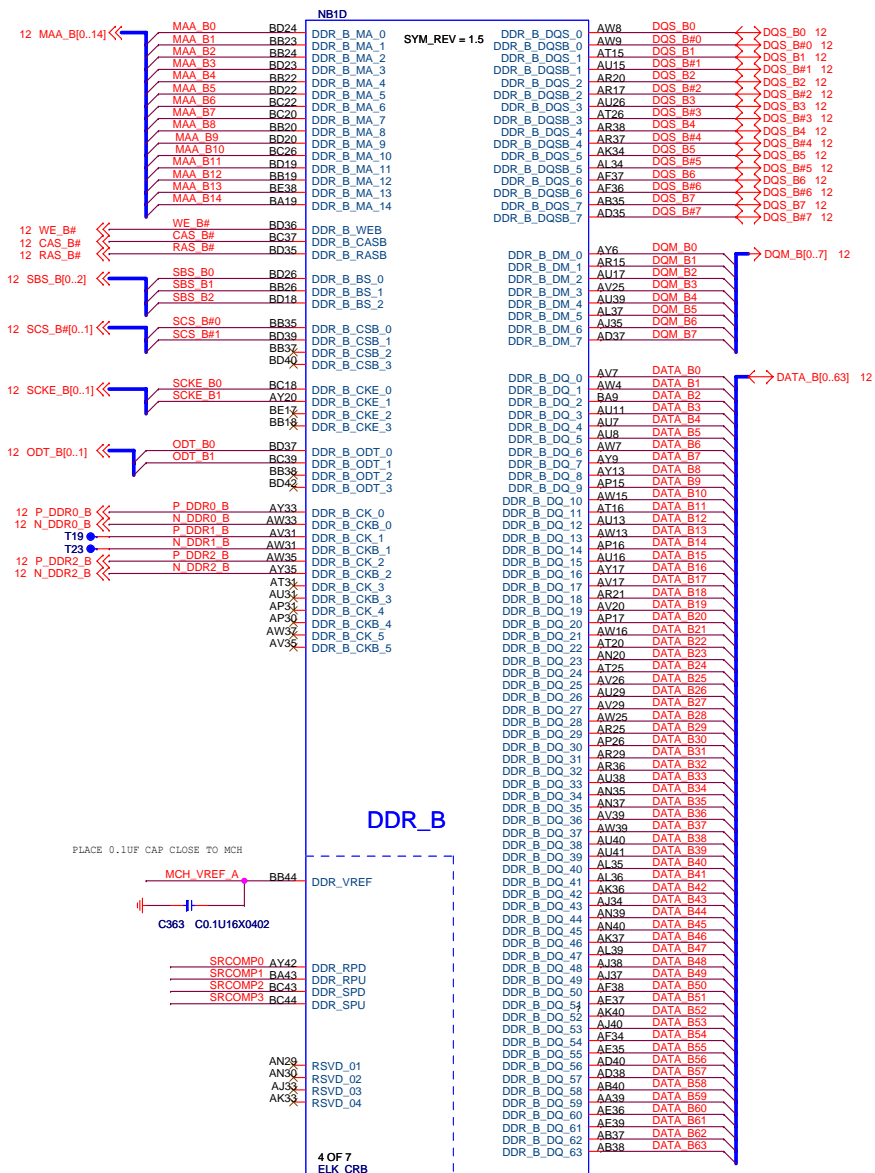
Place near each VDD_CK Pins



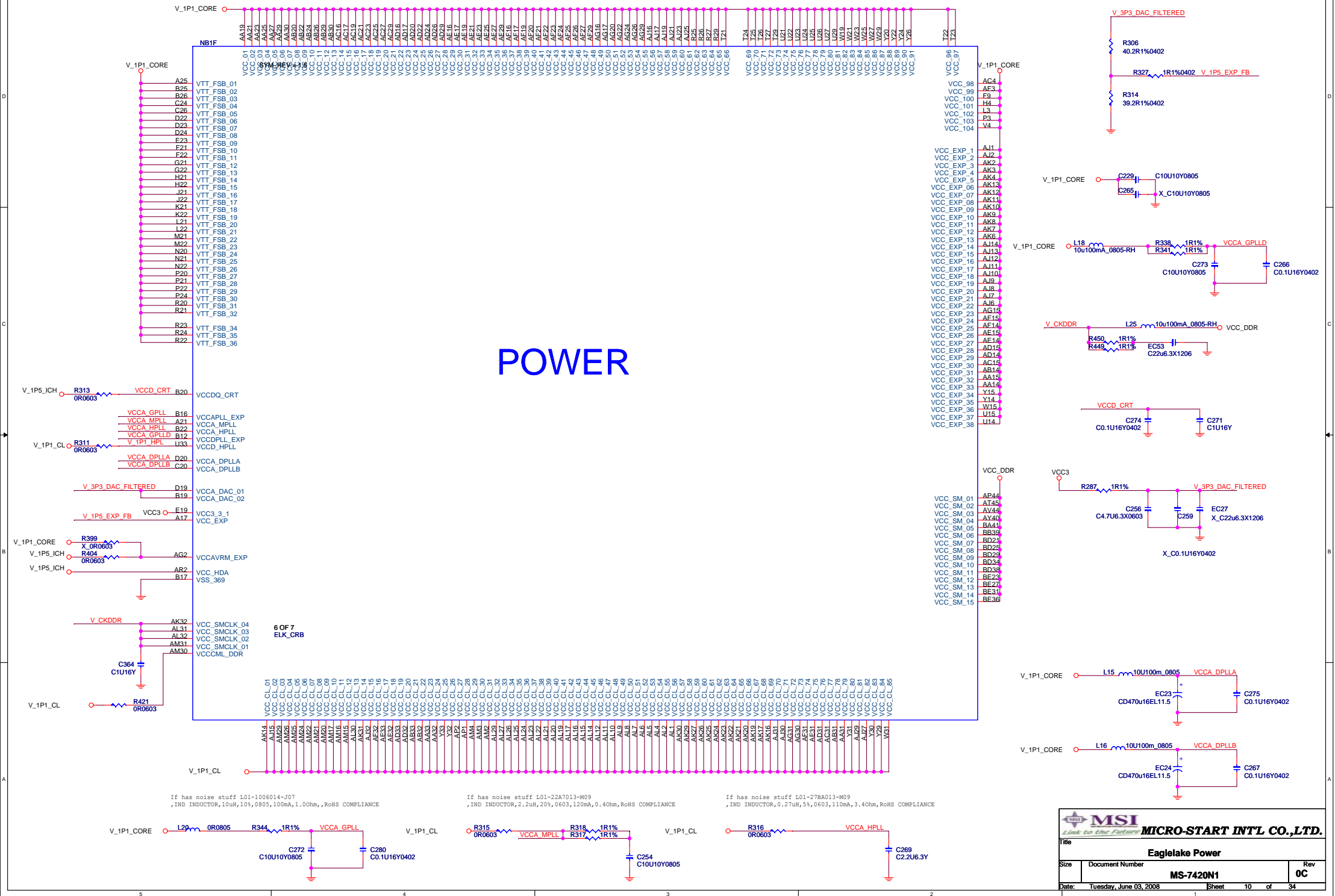
FS ₁ C ¹ B0b7	FS ₁ B ¹ B0b6	FS ₁ A ² B0b5	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Reserved

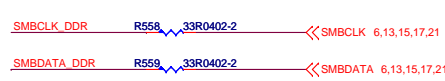
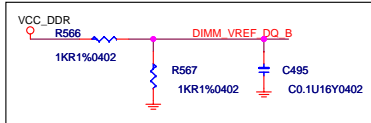
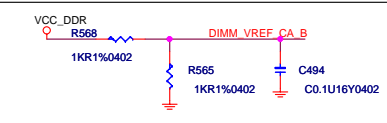
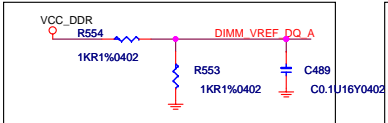
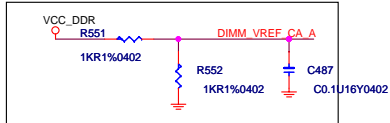
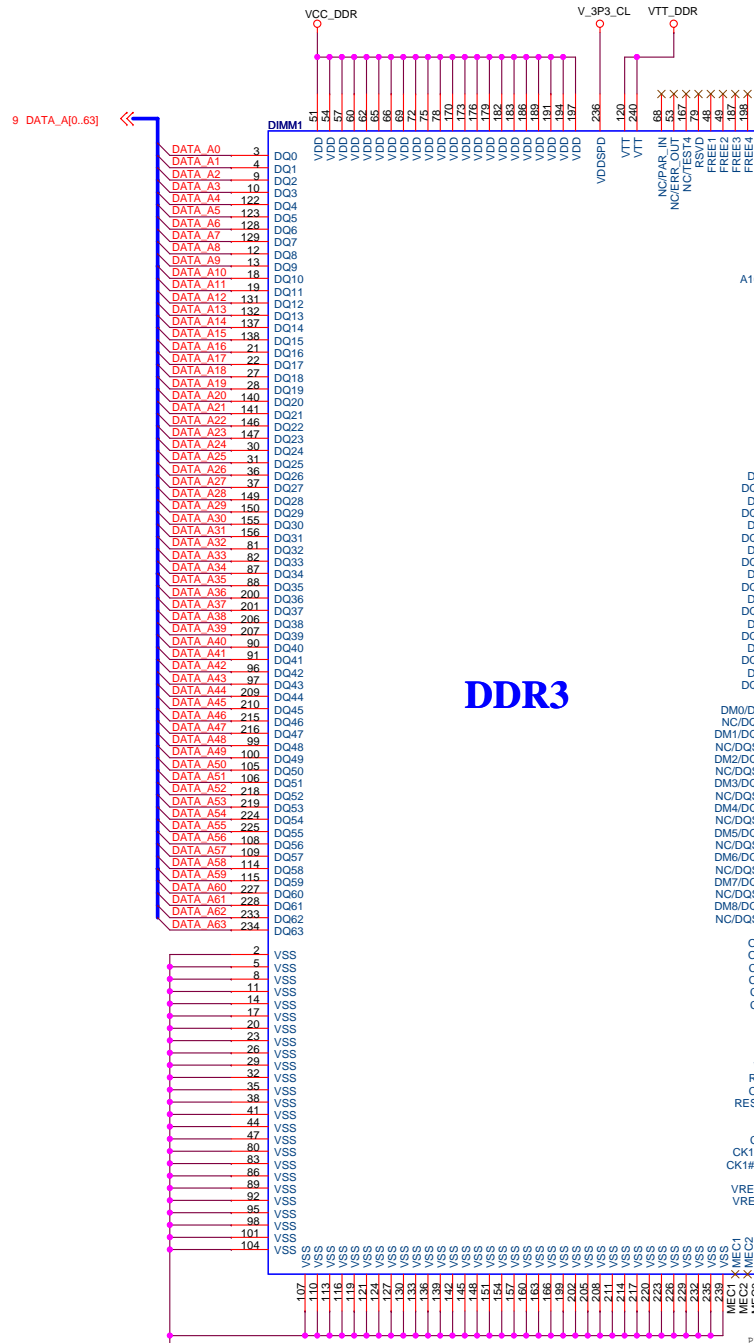




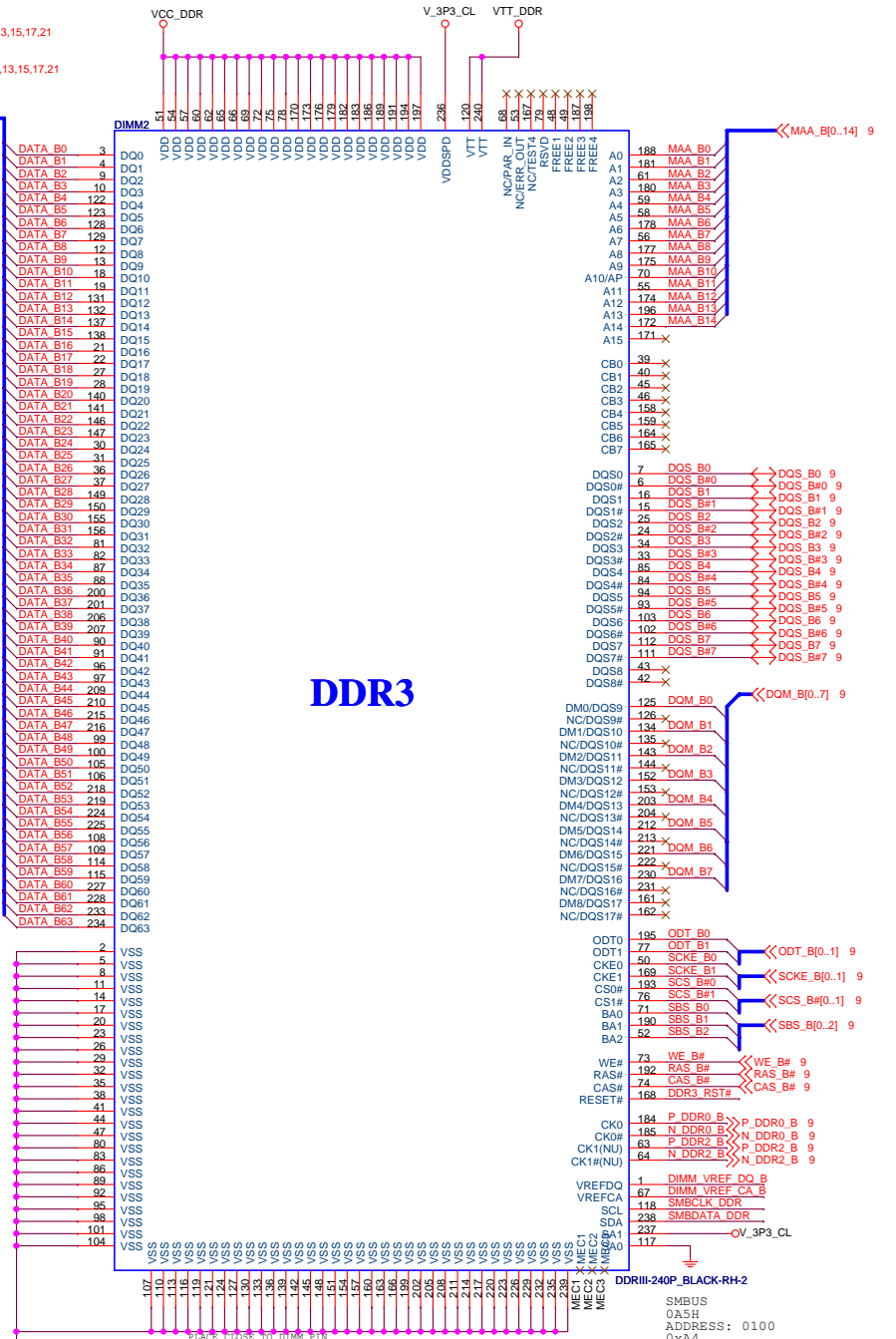


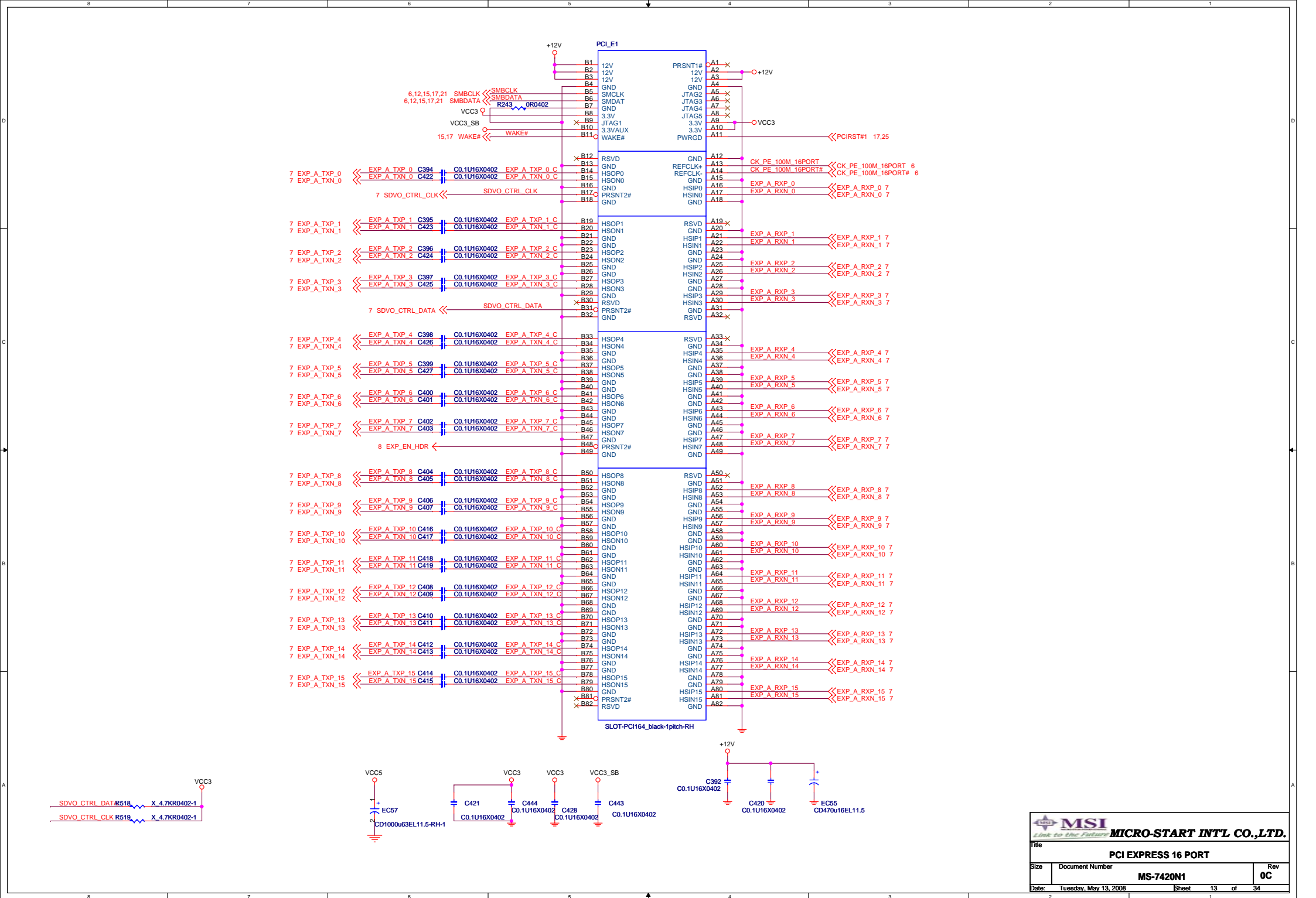
POWER

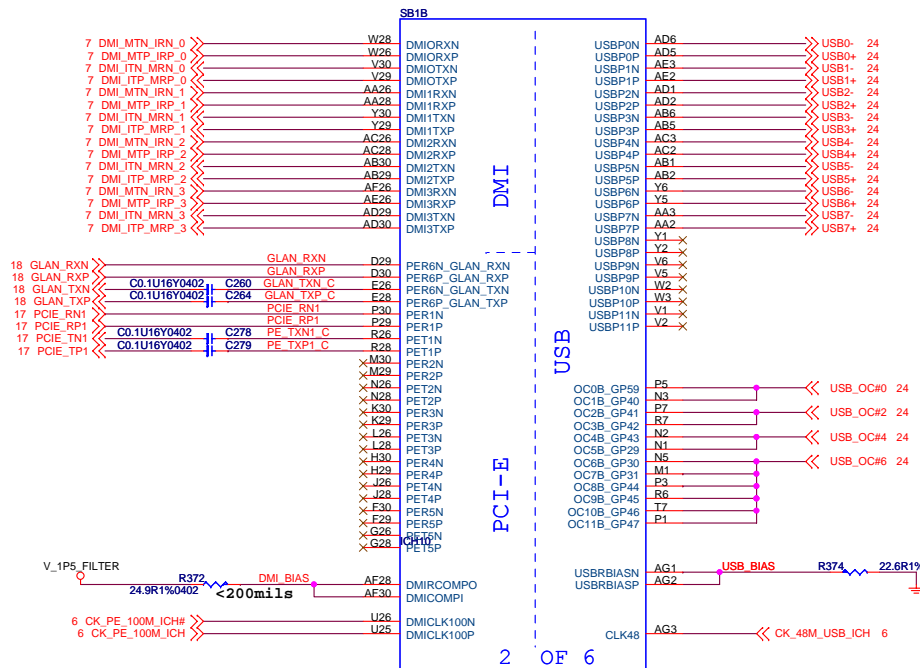
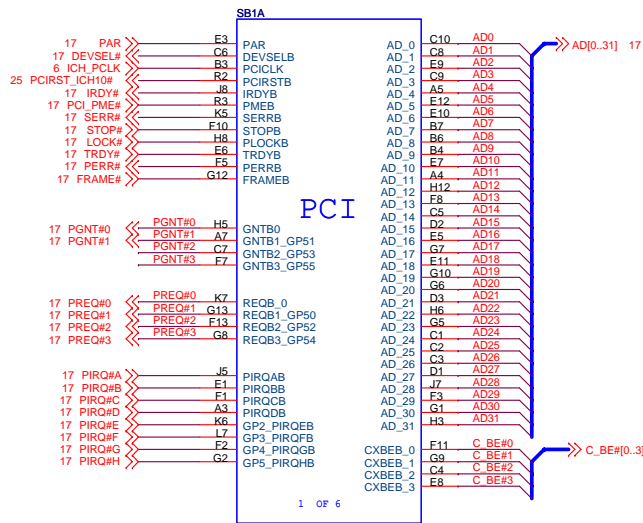




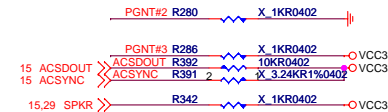
9 DATA_B[0..63]



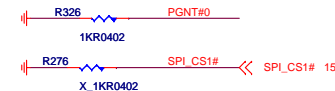




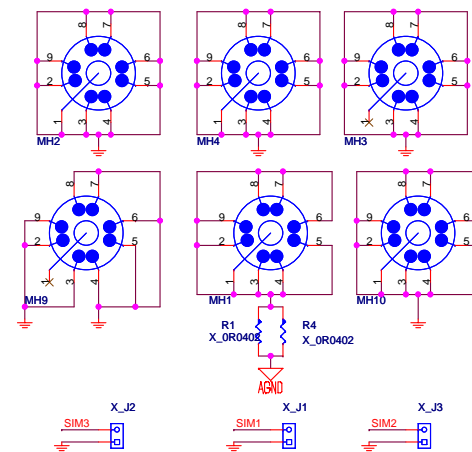
ICH10 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	EN	DIS	Danbury Tec.
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)



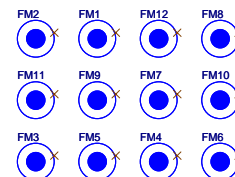
BOOT SELECT STRAPS			
BOOT DEVICE	GNT#0	SPI_CS1#	
FWH	1	1	
SPI	0	X	(Default)
PCI	1	0	



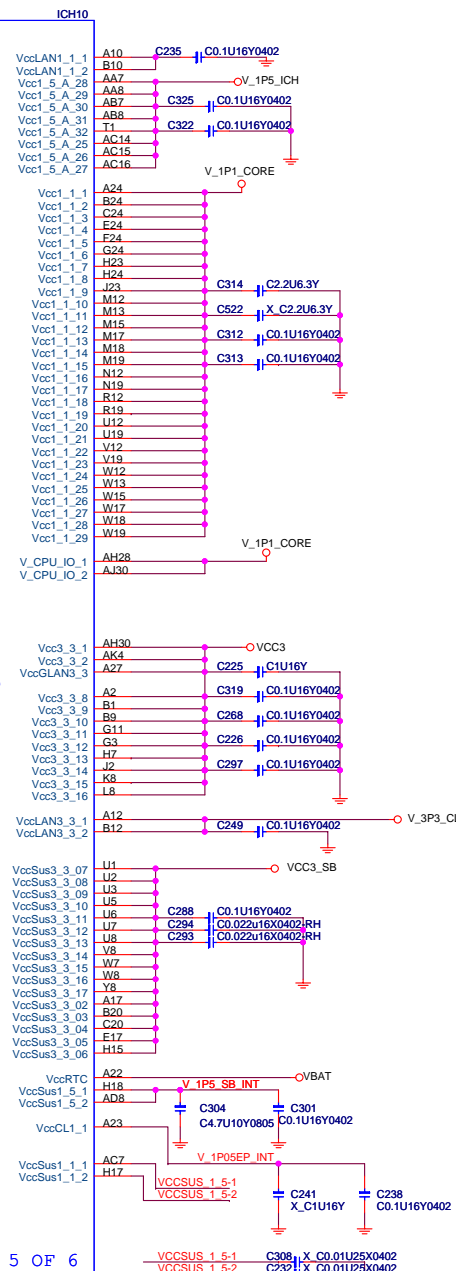
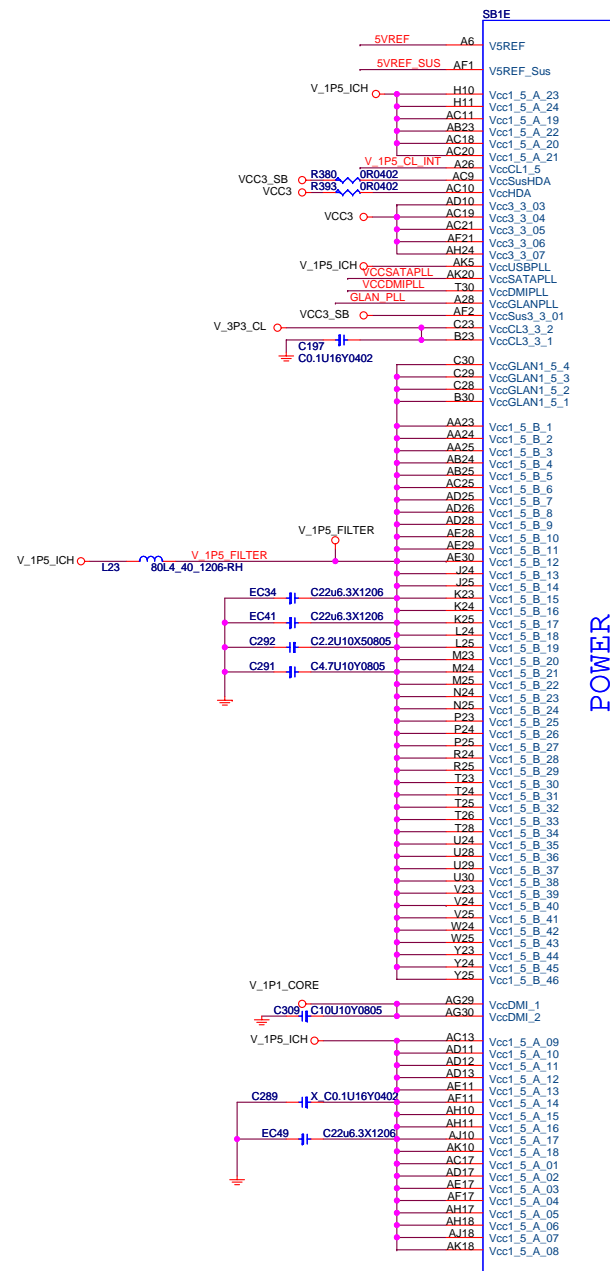
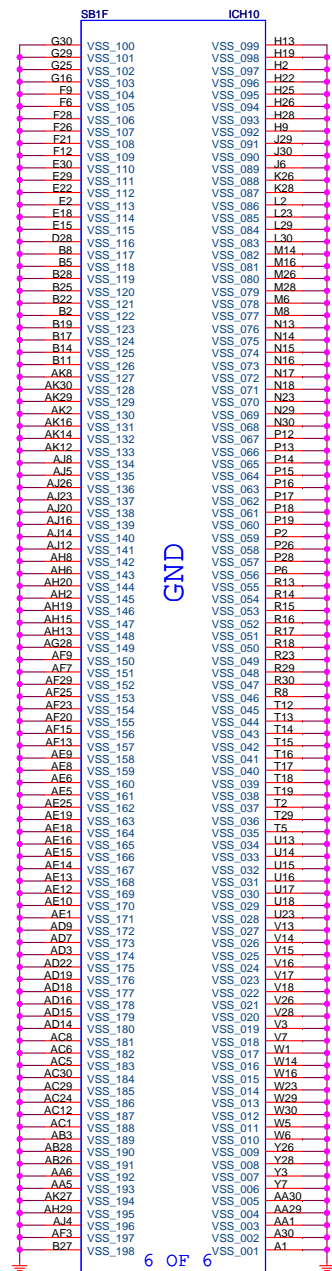
Mounting Holes



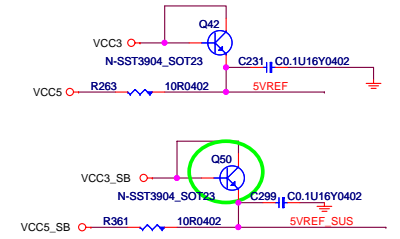
Optics Orientation Holes



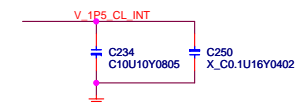
MICRO-START INTL CO.,LTD.			
Title INTEL ICH10 PART1			
Size	Document Number MS-7420N1		Rev 0C
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5VREF & 5VREF_SUS Sequencing Circuit



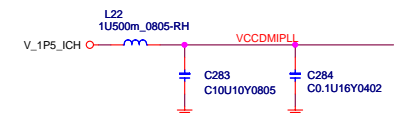
V_1P5_CL decoupling



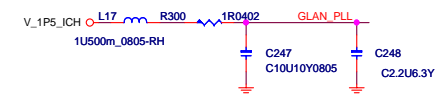
VCCSATAPLL



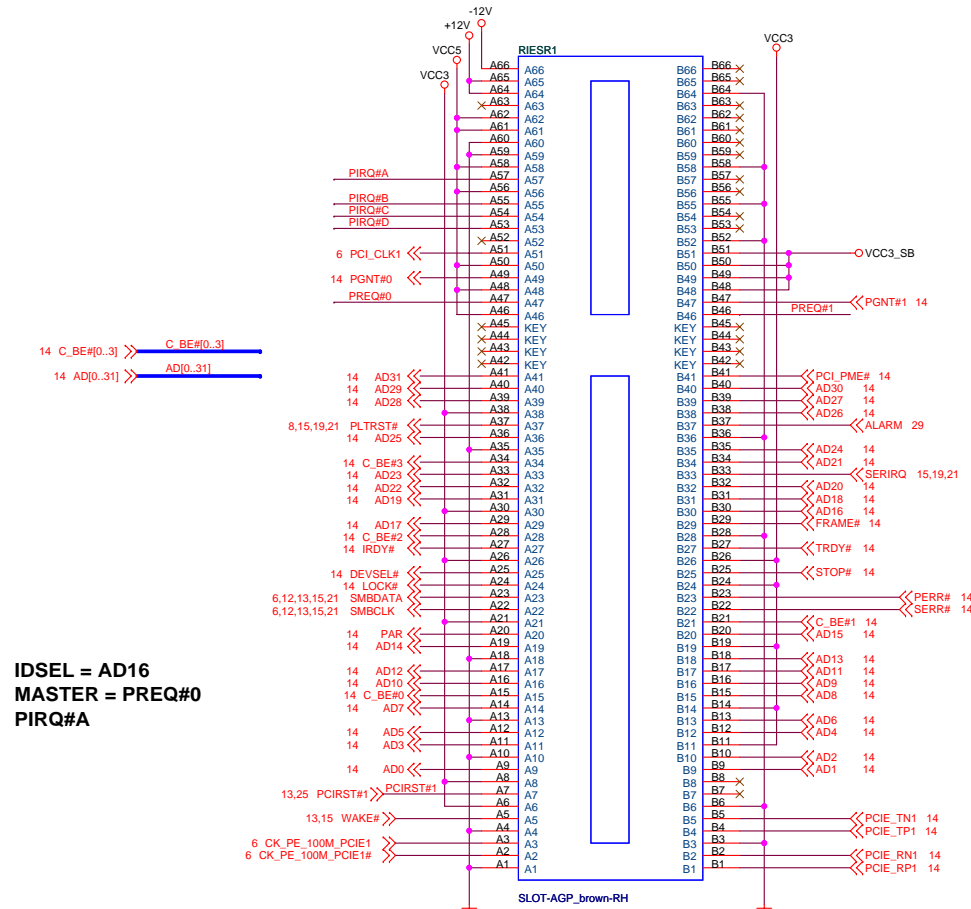
VCCDMIPLL



GLAN_PLL



LE riser card interface

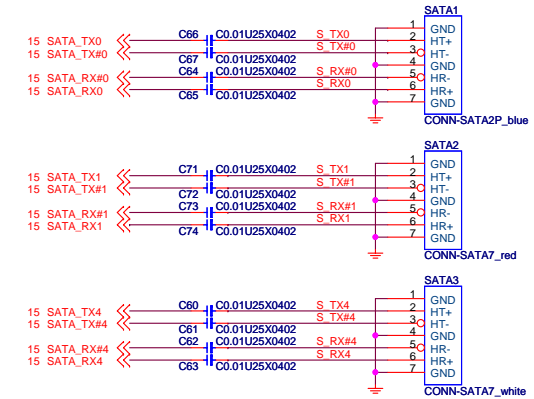


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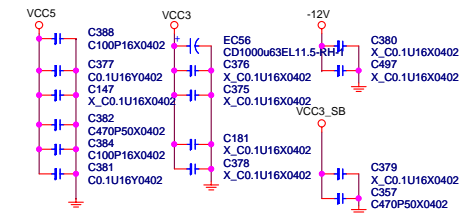
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

```

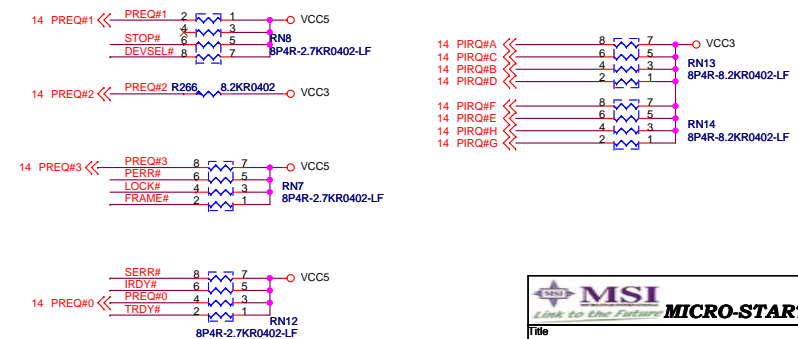
SERIAL ATA CONNECTOR BLOCK



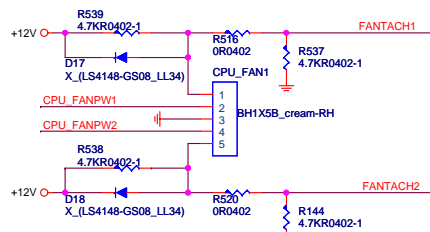
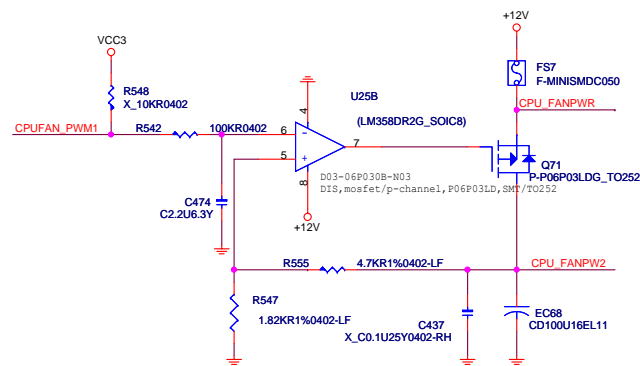
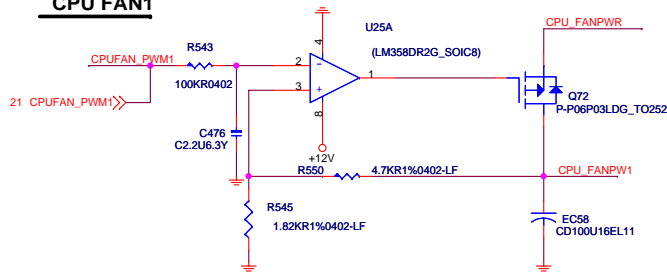
PCI SLOT DECOUPLING CAPACITORS



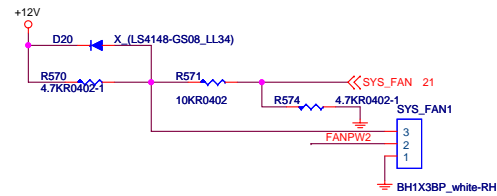
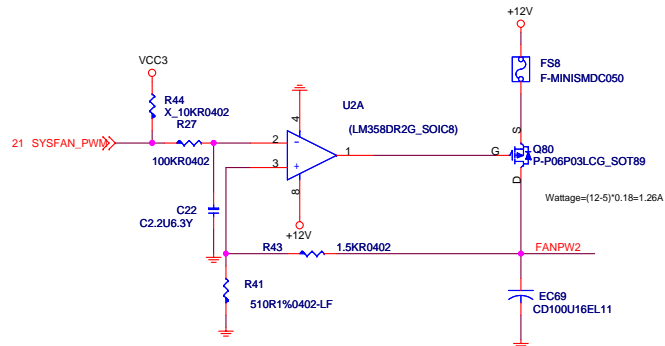
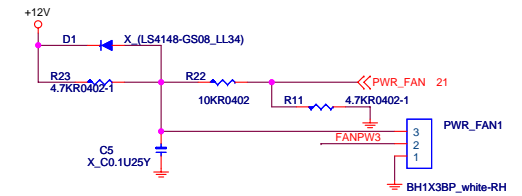
PCI PULL-UP / DOWN RESISTORS



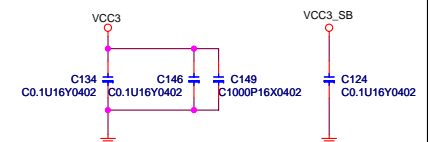
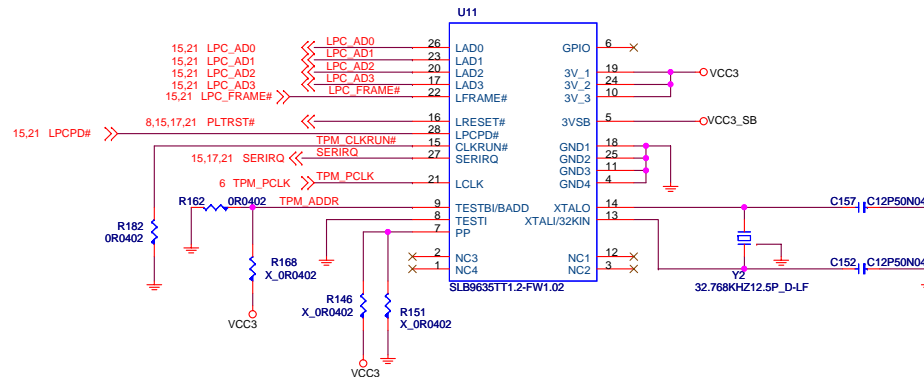
CPU FAN2



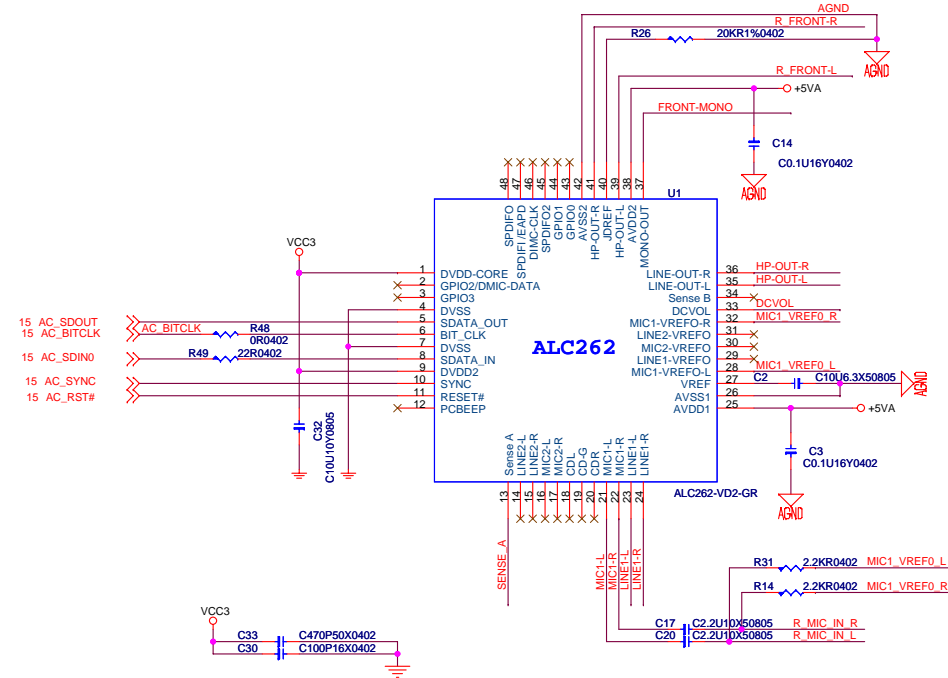
SYS FAN

[illegible]

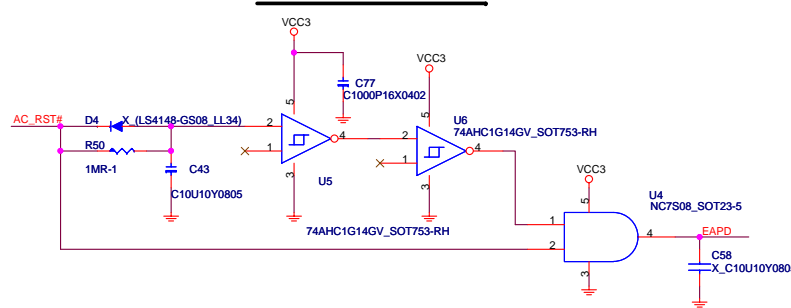
IO Address:0x02E



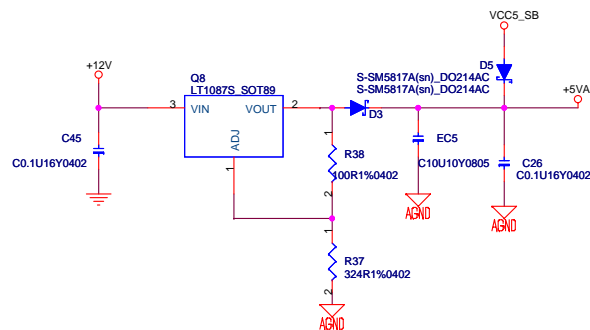
RELTEK HD ALC262VD2



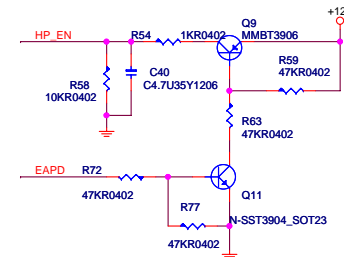
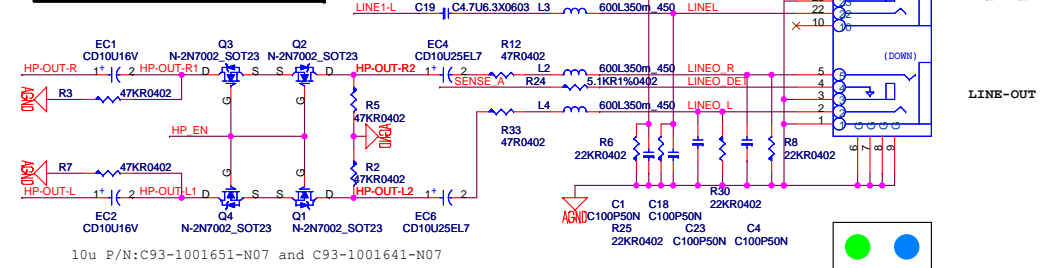
POP noise circuit



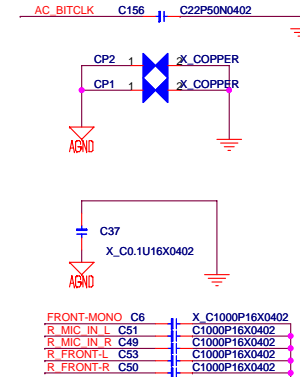
Audio CODEC REGULATOR



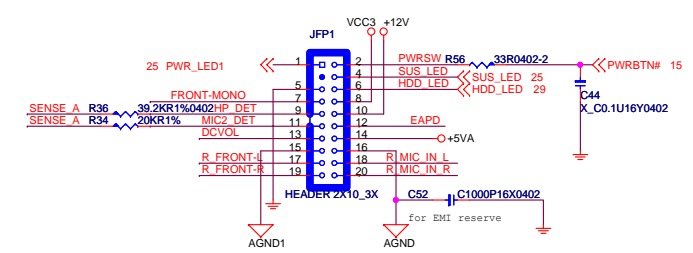
Smooth POP noise circuit



For EMI reserve

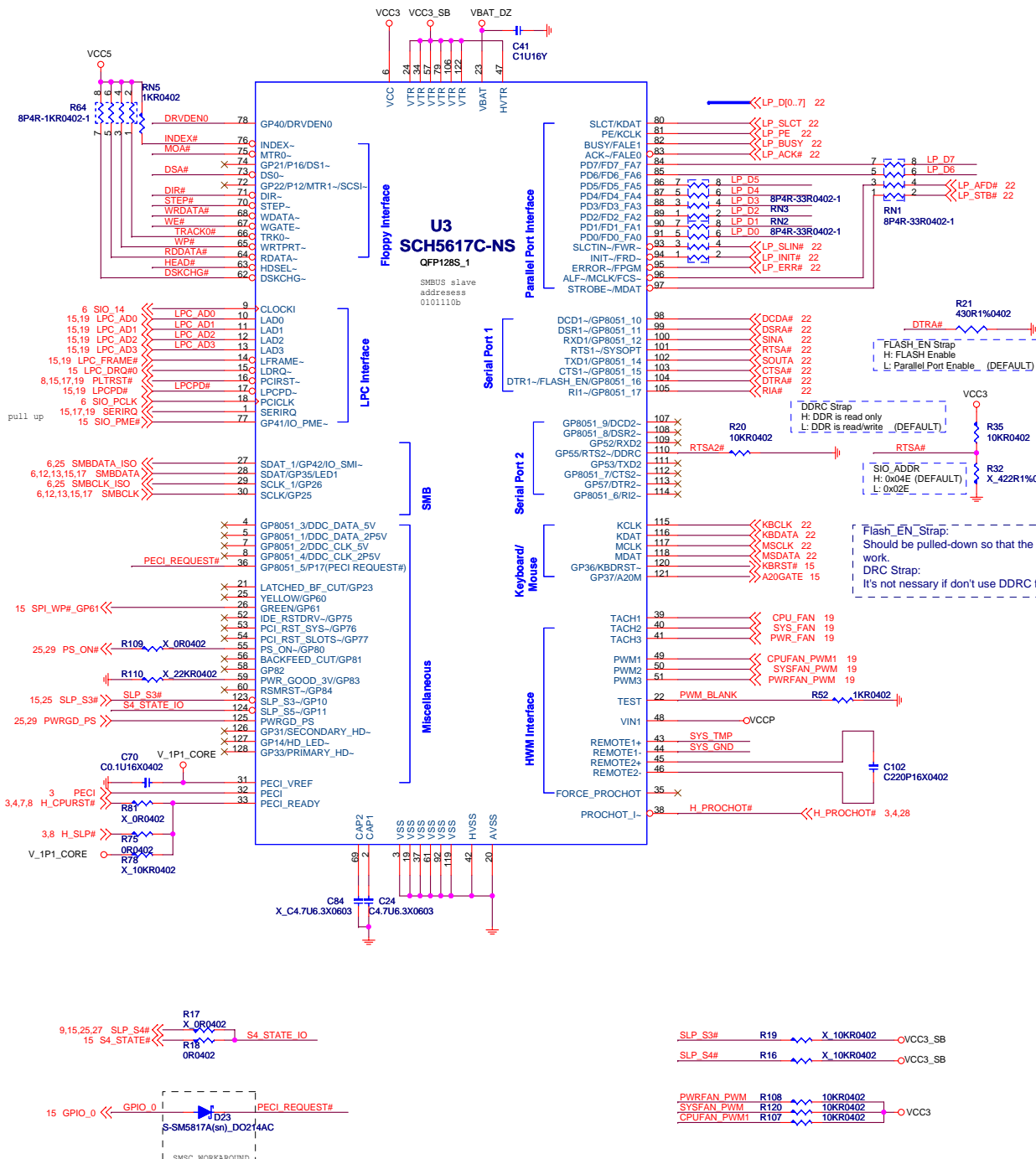


For Front Panel

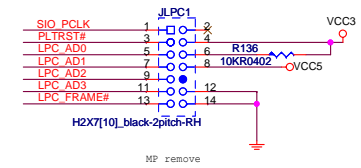


JFP1

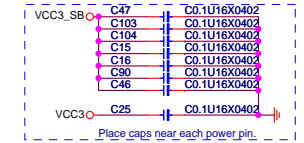
1	PWR_LED	POW_SW	2
3	NC	SLP_LED	4
5	GND	HDD_LED	6
7	Mono	VCC3	8
9	HP_DET	+12V	10
11	MIC_DET	EAPD	12
13	DCVOL	+5VA	14
15	AGND1	AGND	16
17	FRONT_L	MIC_L	18
19	FRONT_R	MIC_R	20



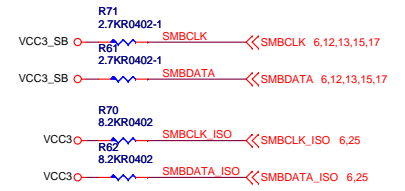
Debug port



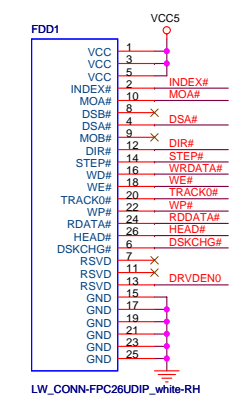
SIO power decoupling



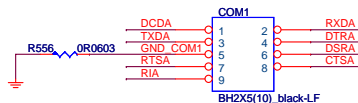
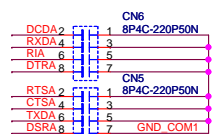
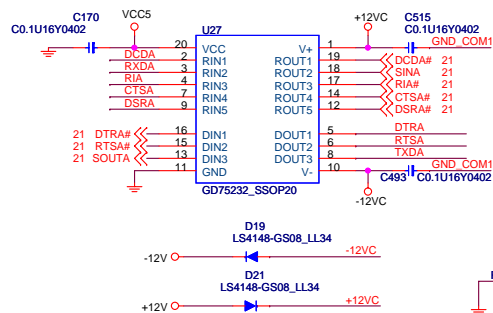
SMBUS pull-up resistor



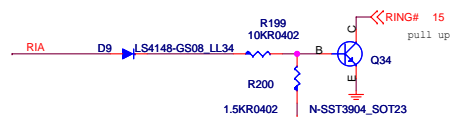
1/2" Notebook type



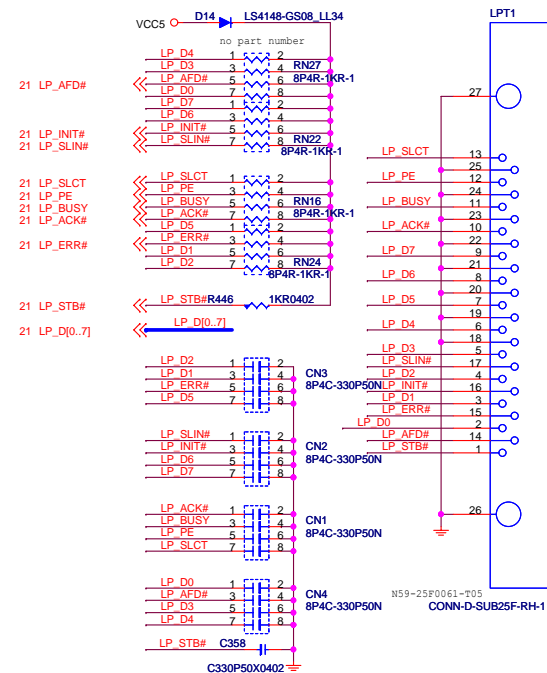
SERIAL PORT 1



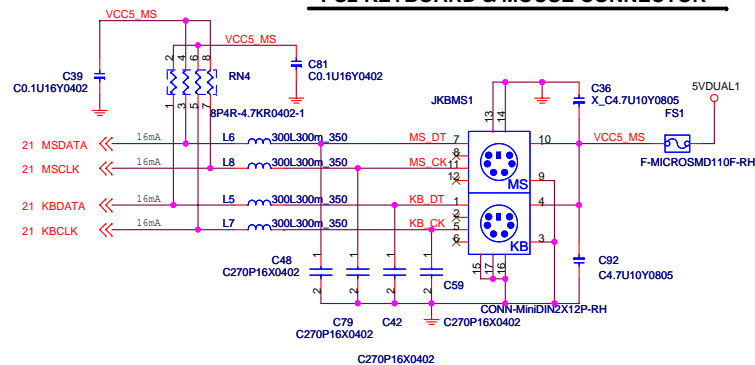
Wake On Modem Header



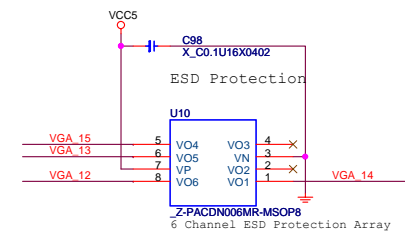
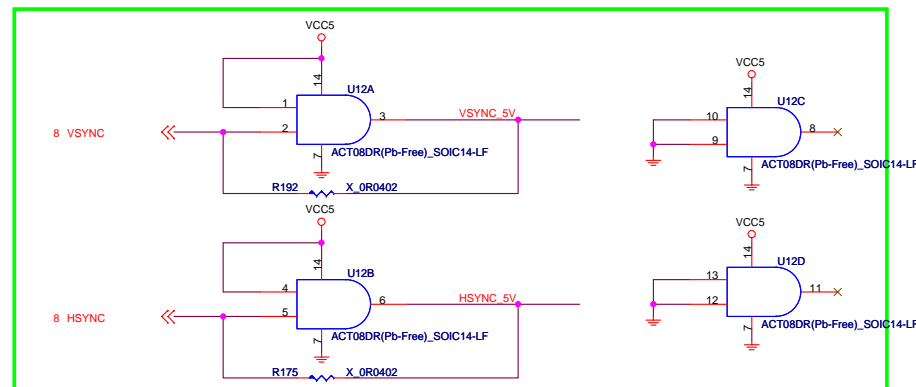
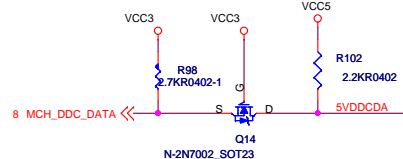
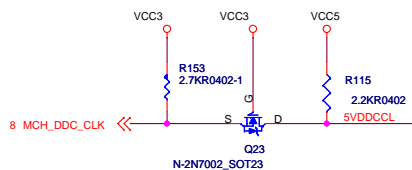
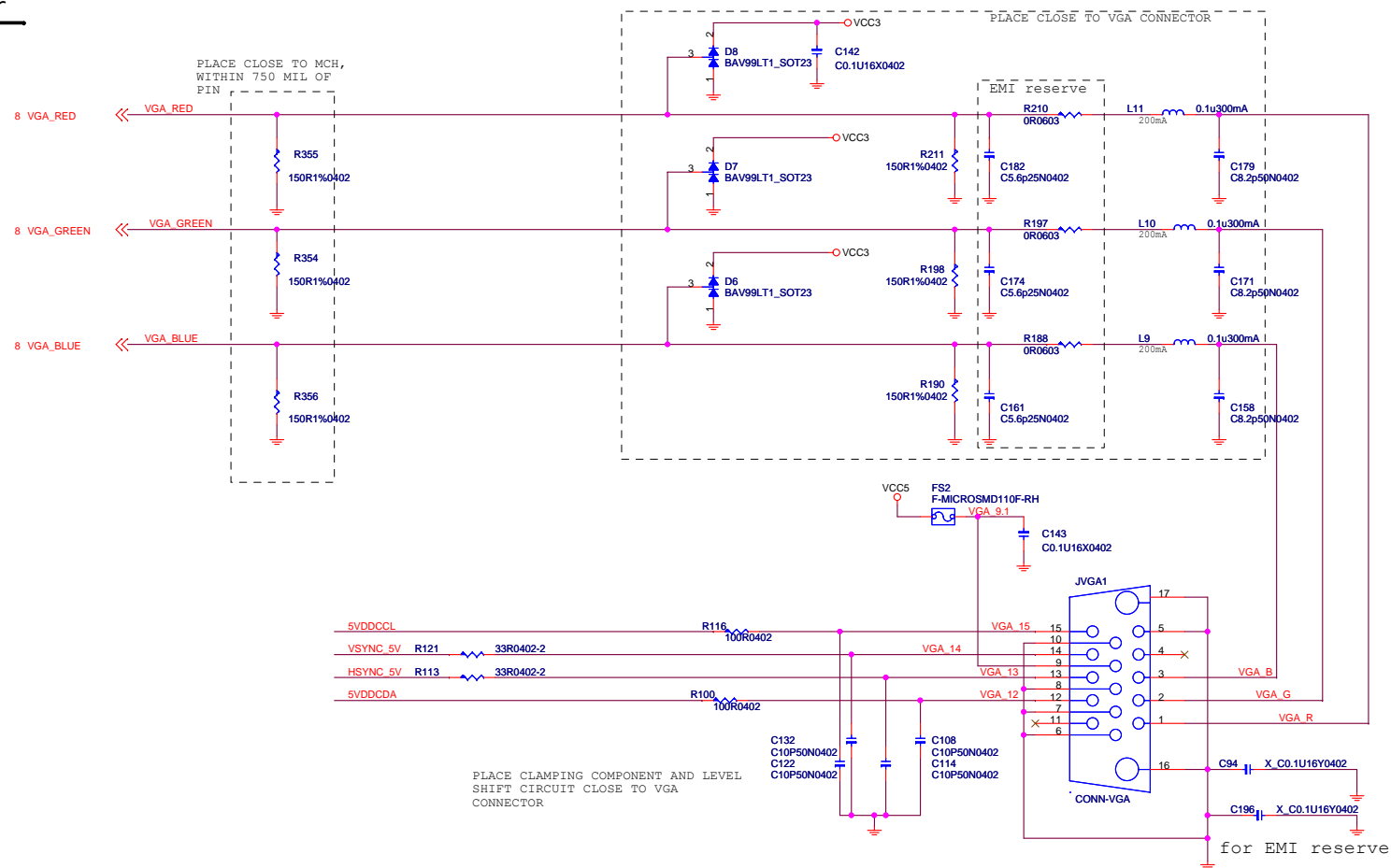
PARALLAL PORT



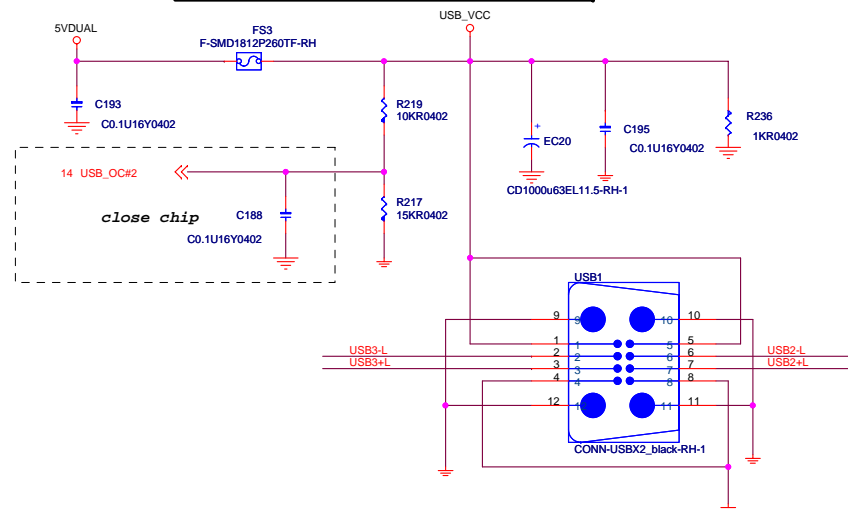
PS2 KEYBOARD & MOUSE CONNECTOR



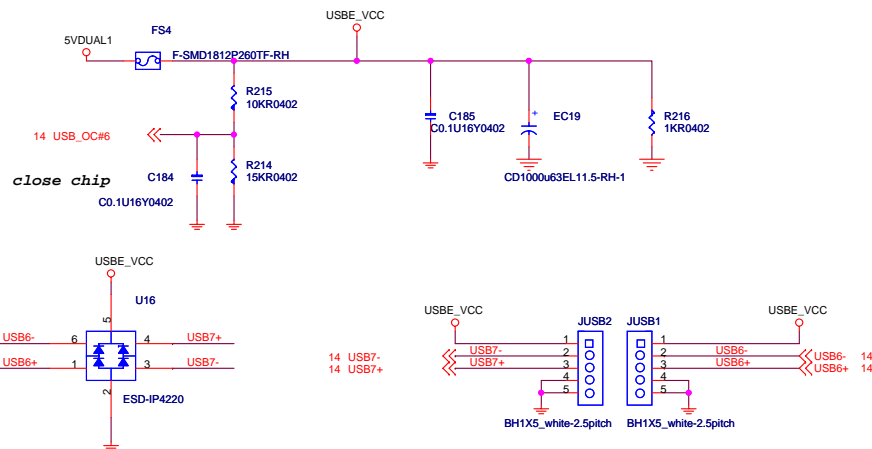
Video Connector



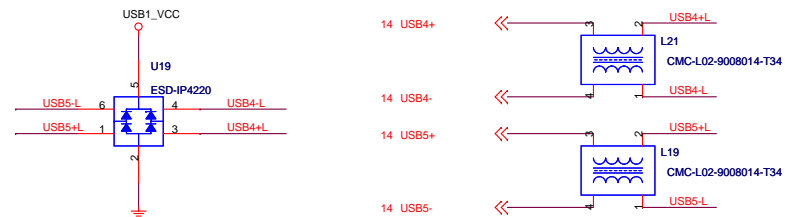
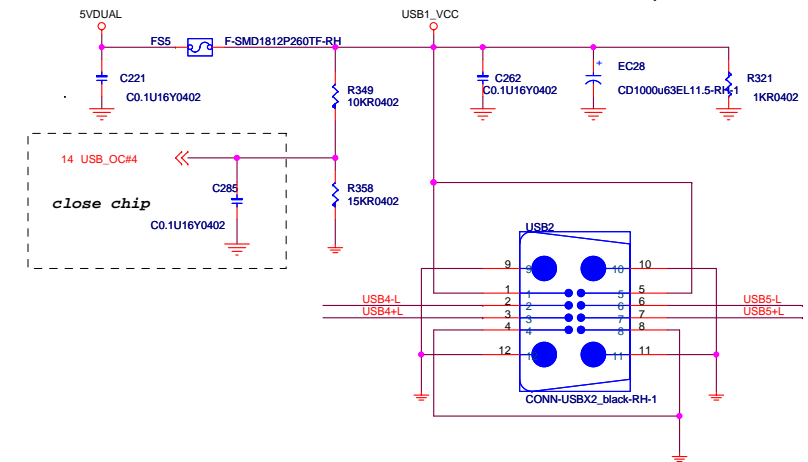
REAR PANEL USB PORT 2,3 CONNECTOR



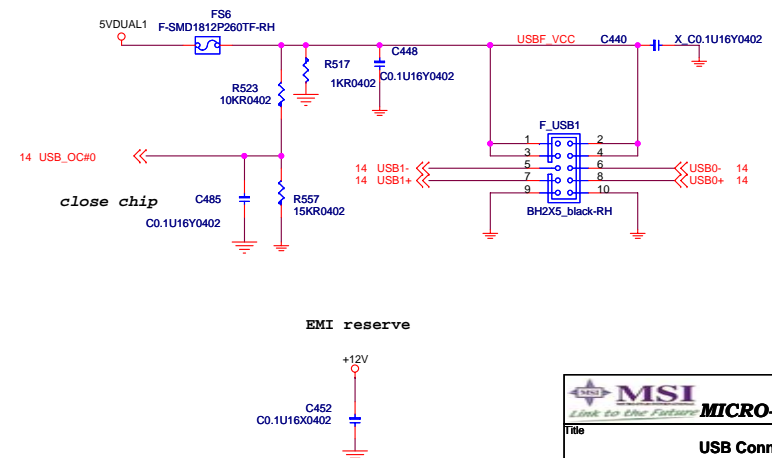
RESERVE EXTERNAL USB PORT 6,7



REAR PANEL USB PORT 4,5 CONNECTOR



FRONT PANEL USB PORT 0,1 CONNECTOR



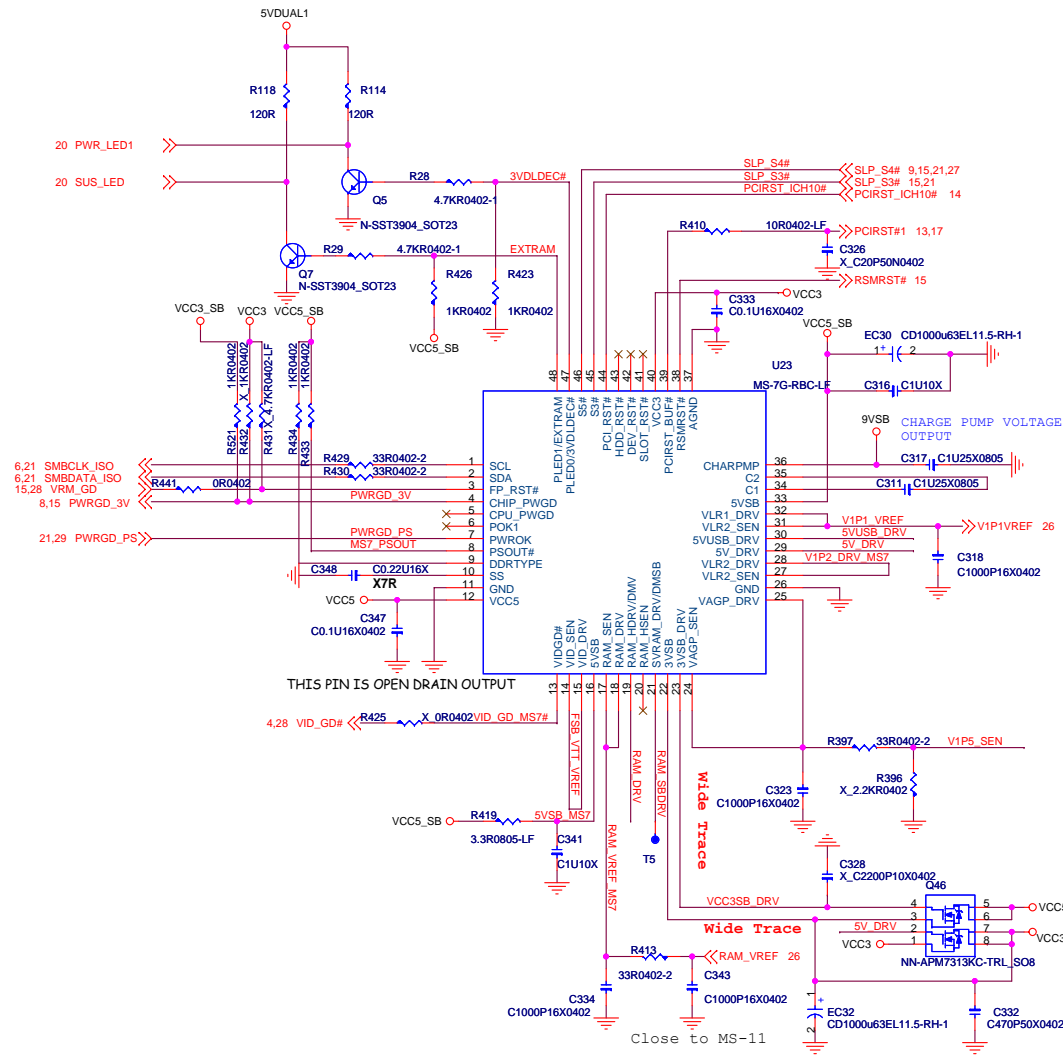
ACPI Controller

VDIMM LINEAR OR PWM SELECT

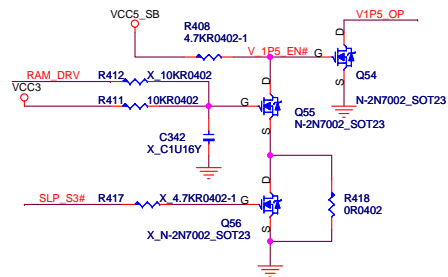
VDIMM MODE EXTRAM
 LINEAR REGULATOR PULL LOW
 PWM REGULATOR PULL HIGH

3VSB MODE SELECT

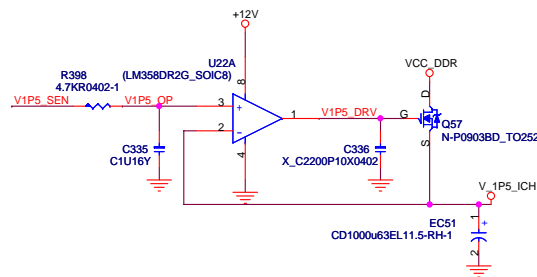
3VSB MODE BVDLDEC#
 SINGLE MOSFET PULL HIGH
 DUAL MOSFET PULL LOW



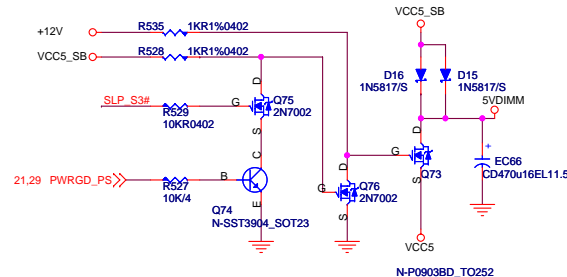
V1P5_SEN S3 power sequency



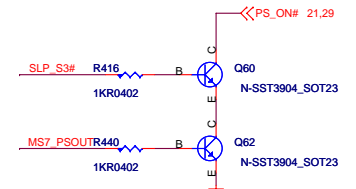
ICH10 1.5V POWER (2.385A)



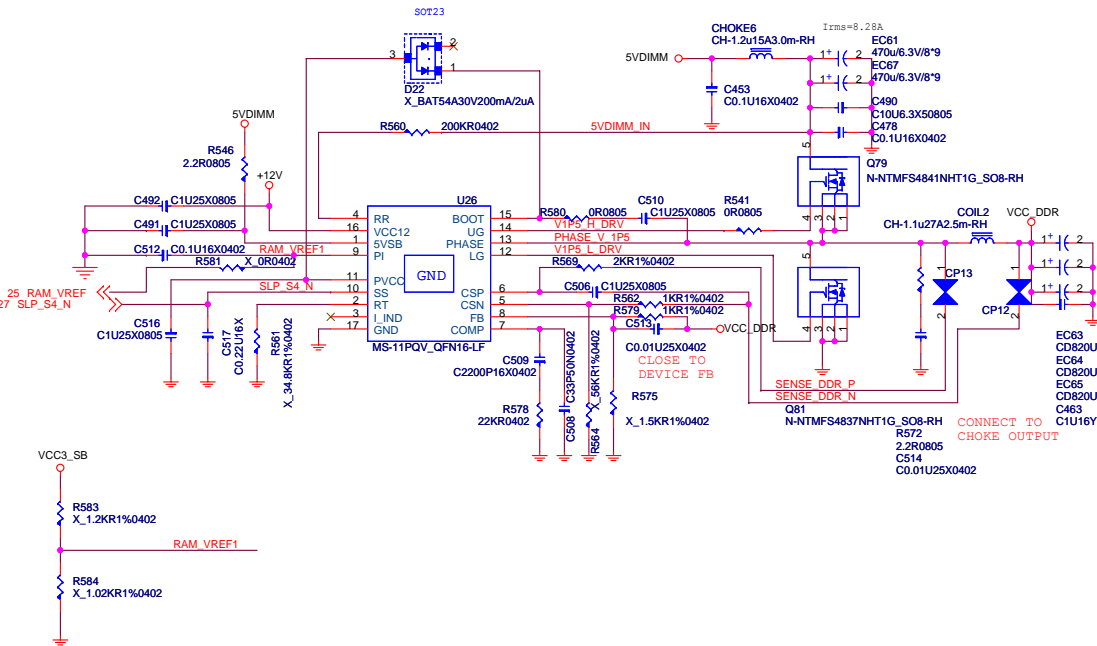
5VDIMM



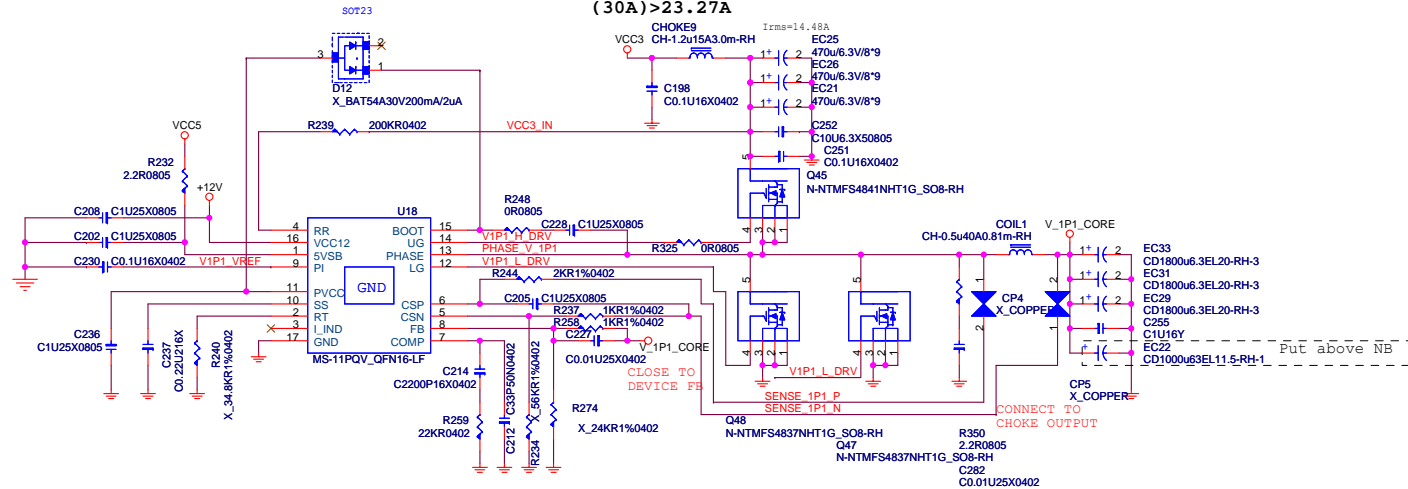
PSON#



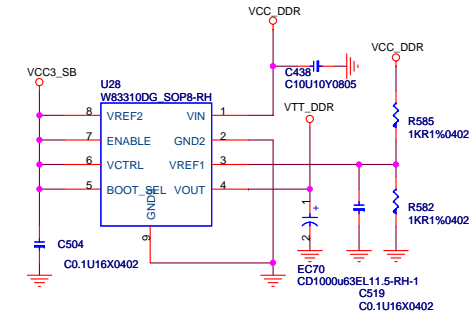
DDRIII 1.5V POWER (18A) > 13.86A



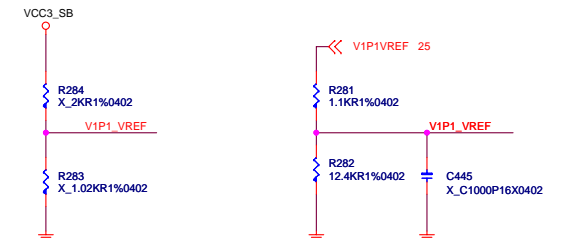
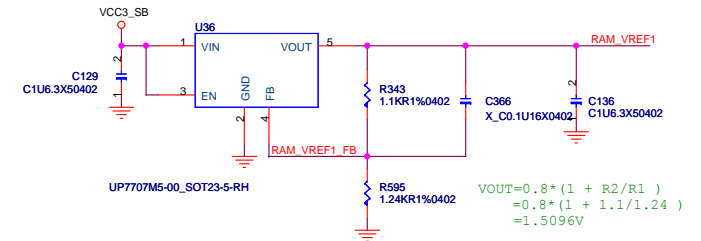
GMCH/ICH10 1.1V POWER (30A) > 23.27A

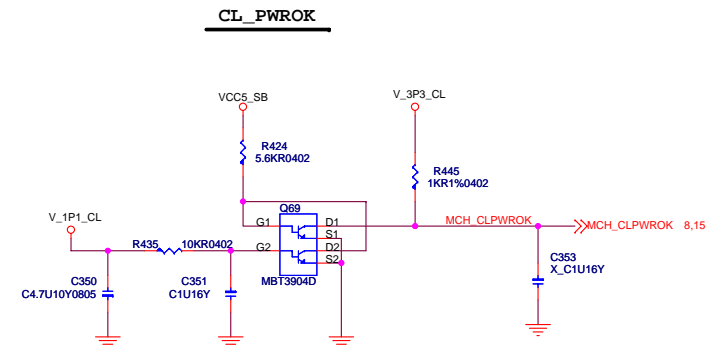
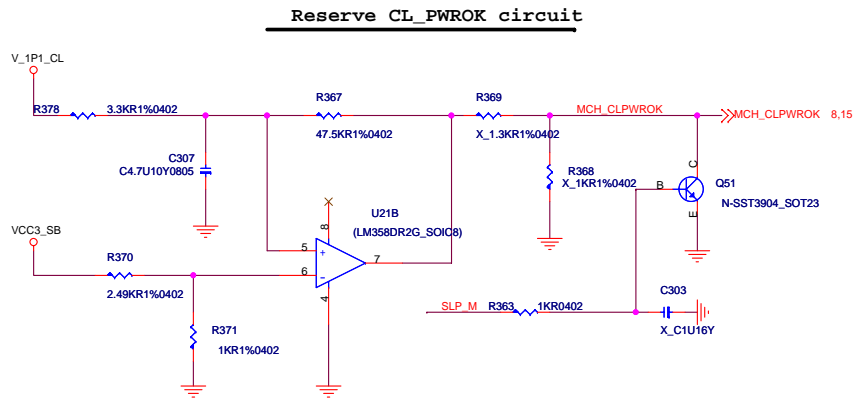
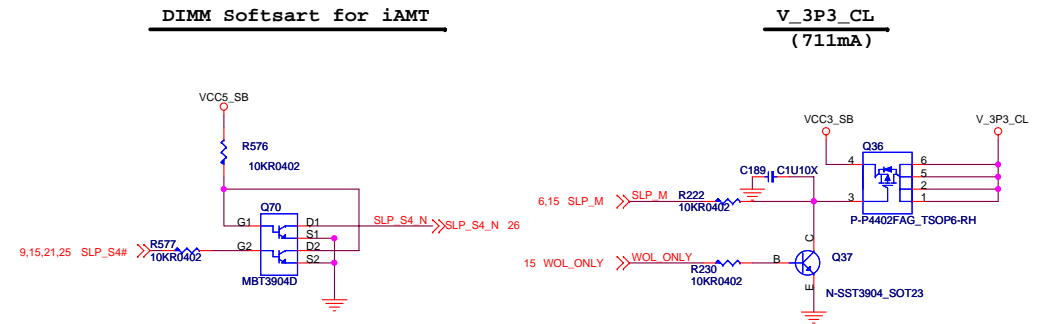
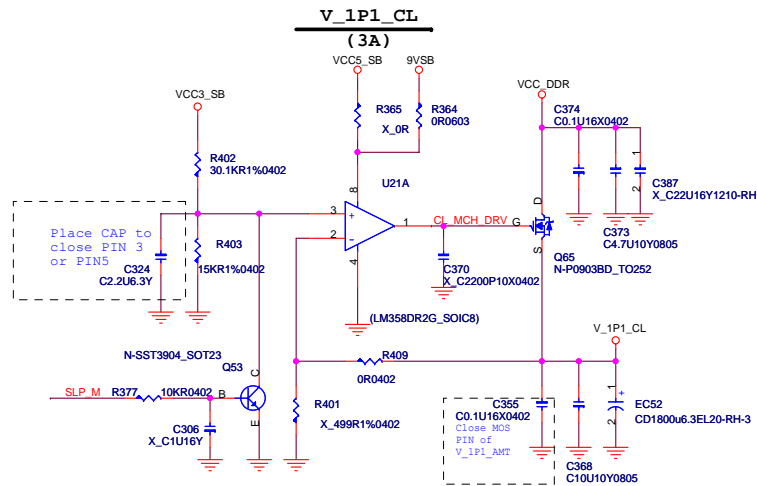


DDR VTT Power (0.83A)



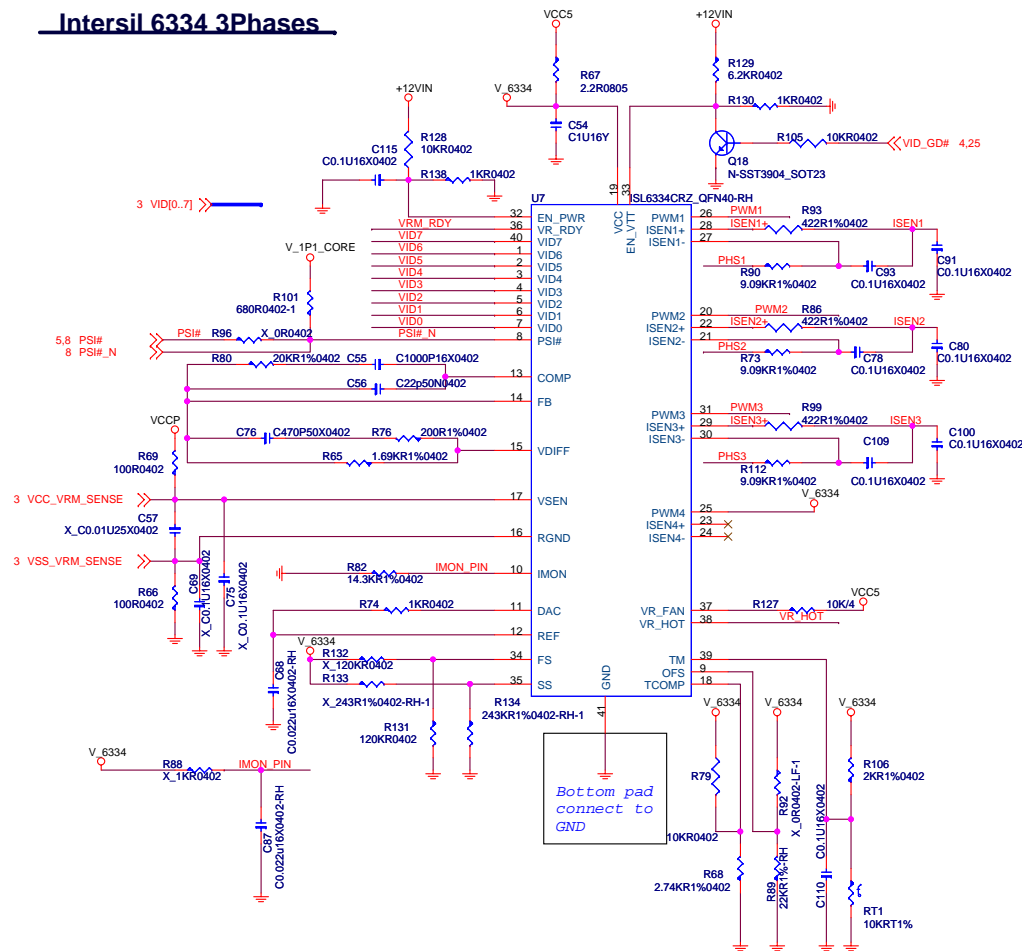
VCC_DDR reference Power



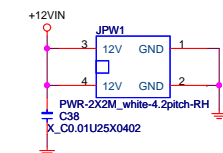


Note:
 SLP_S4#
 AMT Disable-->indicate ACPI S4 state, DRAM power off.
 AMT Enable-->not be asserted ACPI S4 state, DRAM power ON
 SLP_M#
 AMT Enable SLP_M#-->Control the overall power to Intel AMT during ACPI S3-S5.
 S4_SATE#
 AMT Enable-->indication of ACPI S4 state

Intersil 6334 3Phases



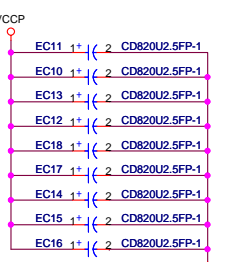
ATX12V Power Connector



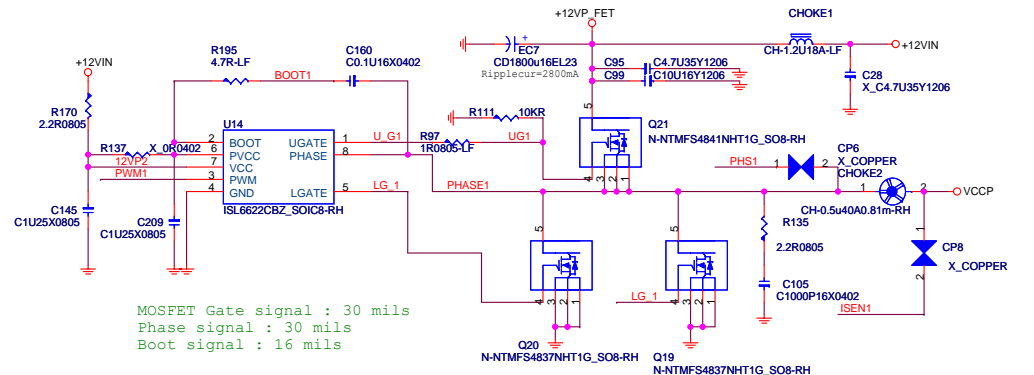
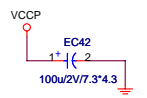
TDK
N7C104K104FT

VR FAN TRIP: 1.69V ~ 80 degC
VR HOT TRIP: 1.44V ~ 90 degC

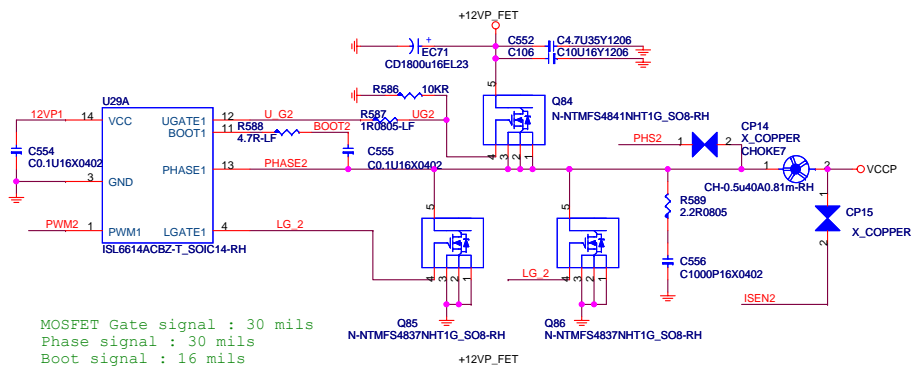
OS-CON Capacitors



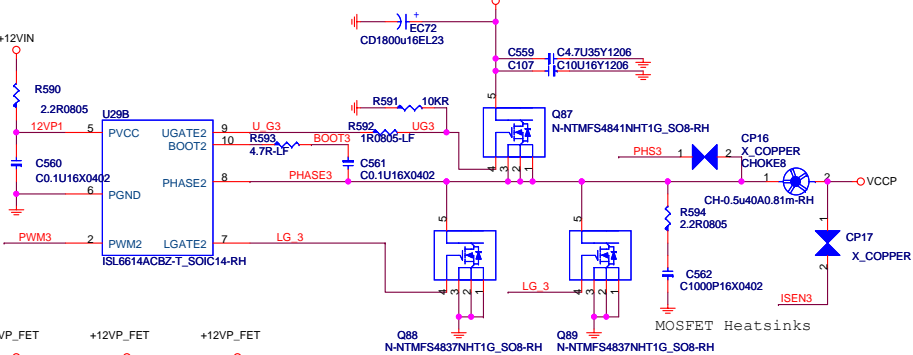
SP Capacitors



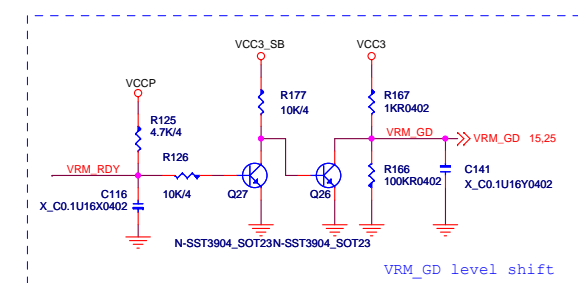
MOSFET Gate signal : 30 mls
Phase signal : 30 mls
Boot signal : 16 mls



MOSFET Gate signal : 30 mls
Phase signal : 30 mls
Boot signal : 16 mls



MOSFET Heatsinks



VRM_GD level shift

MICRO-START INT'L CO.,LTD.		
Intersil 6334 3Phases		
Size	Document Number	Rev
	MS-7420N1	0C
Date:	Tuesday, June 03, 2008	Sheet 28 of 34

VCC5

Ic=200mA
Vbe=5V
Vceo=40V

R57 1KR0402

Q10

R53 4.7K R0402-1
P-MMBT3906LT1G_SOT23-RH

R55 120R0402

15 SATA_LED#

20 HDD_LED

17 ALARM

14.15 SPKR

VCC5

BZ1 BUZZER-LF

D13 LS4148-GS08_LL34

RN15

8P4R-470R0402-LF

Q49 N-SST3904_SOT23

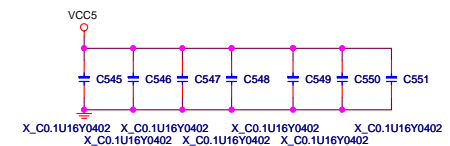
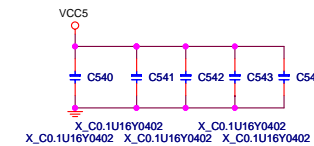
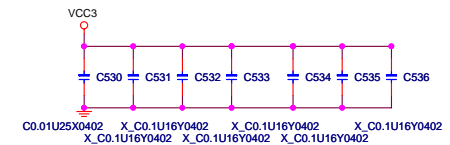
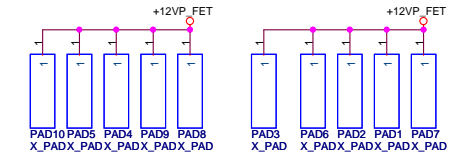
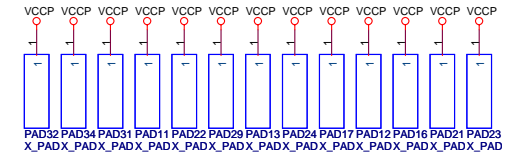
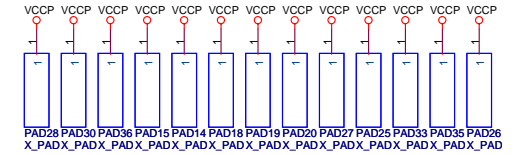
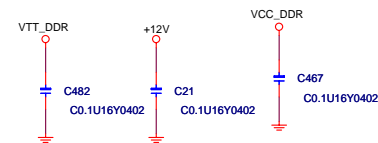
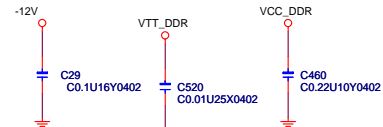
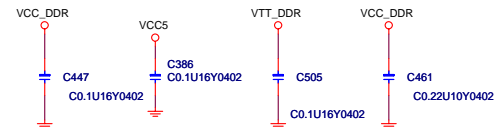
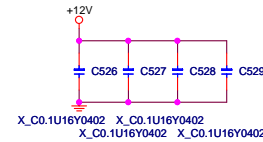
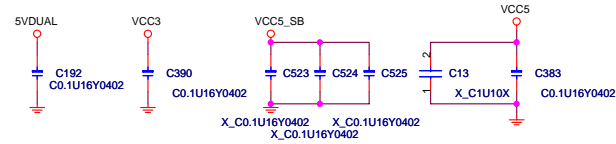
R359 2.7K

C295 X_Co.1U16Y0402

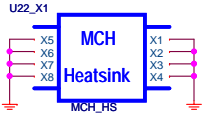
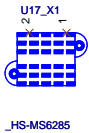
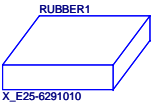
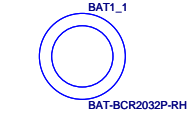
C199 C0.1U16V0402

Place near CK_48M_USB_ICh for EMI.

V_1P1_CORE
C305 C0.1U16Y040
Place near R643 for EMI.



Auto-BOM Manual Parts



ICH10

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	BMBUSY# function, Pull-up to VCC3 with 10K	VCC3	MUXED	N7
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK21
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 8.2K	VCC3		K6
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 8.2K	VCC3		L7
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 8.2K	VCC3		F2
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 8.2K	VCC3		G2
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AH22
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AK23
GPIO 8	I/O	GPI	Reserve for DDR_PEROK, Pull-up to VCC_DDR with 10K	VCC3_SB	UNMUXED	A20
GPIO 9	I/O	GPO/WOL	WOL_ENABLE/GPIO9, pull-down with 100K	VCC3_SB	MUXED	A18
GPIO 10	I/O	GPI	Detect AUDIO Devices, Pull-up to VCC3_SB with 10K	VCC3_SB	MUXED	C17
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		C16
GPIO 12	I/O	GPO	LAN_DISABLE	VCC3_SB	UNMUXED	A8
GPIO 13	I/O	GPI	SIO_PME# connect to SIO, pull-up VCC3_SB with 10K	VCC3_SB	UNMUXED	A19
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	A9
GPIO 15	I/O	GPO	PCI_STOP# for CK505 IAMT	VCC3_SB	MUXED	C15
GPIO 16	I/O	GPO	FAN switch, pull-up VCC3 with 10K.	VCC3	UNMUXED	M2
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3	MUXED	AH21
GPIO 18	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	K1
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AE20
GPIO 20	I/O	GPO	GTLREF GPO	VCC3	UNMUXED	AF5
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AK25
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AJ24
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull-up VCC3 with 10K(Not Use)	VCC3	MUXED	J3
GPIO 24	I/O	GPO	NC	3.3V_SB	MUXED	A14
GPIO 25	I/O	GPO	CPU_STOP# for CK505 IAMT	3.3V_SB	UNMUXED	B18
GPIO 26	I/O	GPO	S4 STATE#	3.3V_SB		C11
GPIO 27	I/O	GPO	NC	3.3V_SB		A11
GPIO 28	I/O	GPO	NC	3.3V_SB		G18
GPIO 29	I/O	OC5#	OC#4 connect to USB connector	3.3V_SB		N1
GPIO 30	I/O	OC6#	OC#6 connect to USB connector	3.3V_SB		N5
GPIO 31	I/O	OC7#	OC#6 connect to USB connector	3.3V_SB		M1
GPIO 32	I/O	GPO	PROHOT# for NEC Economy mode	VCC3	UNMUXED	K2
GPIO 33	I/O	GPO	Pull-up to VCC3 with 4.7K through JC11 Jumper. (Default)	VCC3	UNMUXED	AF6
GPIO 34	I/O	GPO	NC	VCC3	UNMUXED	AH5
GPIO 35	I/O	GPO	Clear password	VCC3		L1
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE21
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AE22
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AK24
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH23
GPIO 40	I/O	OC1#	OC#0 connect to USB connector	3.3V_SB		N3
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	3.3V_SB		P7
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	3.3V_SB		R7
GPIO 43	I/O	OC4#	OC#4 connect to USB connector	3.3V_SB		N2
GPIO 44/45	I/O	OC8/9#	OC#6 connect to USB connector	3.3V_SB		P3/R6
GPIO 46/47	I/O	OC10/11#	OC#6 connect to USB connector	3.3V_SB		T7/P1
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD20
GPIO 49	I/O	GPO	DMI strapping, pull-down 2.2K to GND	VCC3		AJ25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 2.7K	VCC5	MUXED	G13
GPIO 51	I/O	GNT1#	GNT1#	VCC5	MUXED	A7
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 8.2K	VCC5	MUXED	F13
GPIO 53	I/O	GNT2#	GNT2#	VCC3	MUXED	C7
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 2.7K	VCC5	MUXED	G8
GPIO 55	I/O	GNT3#	GNT3#(Not Use)	VCC3	MUXED	F7
GPIO 56	I/O	GPI	Clear password, pull-up to VCC3_SB with 10K.	3.3V_SB	MUXED	F16
GPIO 57	I/O	GPI	Pull-up to VCC3_SB with 10K directly for TPM_PP	3.3V_SB	MUXED	C12
GPIO 58	I/O	SPI_CS1	SPI_CS#(Not Use), SPI_CS1_F#(Not Use)	3.3V_SB	MUXED	F23
GPIO 59	I/O	OC0#	OC#0 connect to USB connector	3.3V_SB		P5
GPIO 60	I/O	LINKALERT	LINKALERT# pull-up to VCC3_SB with 10K	3.3V_SB		F18

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
Riser slot (PCI1)	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDR2 DIMM Configuration

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A2/SCLK_A2#
DIMM 2	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#

SIO - SMSC-5617C Configuration

PIN NAME	PIN#	USAGE	Input/Output
GP41	77	SIO_PME#	OUTPUT
GP25	30	SMBCLK	INPUT
GP26	29	SMBCLK_ISO	INPUT
GP35	28	SMBDATA	OUTPUT
GP42	27	SMBDATA_ISO	OUTPUT

SMBus Distribution

SMBus	Power	Load
SMBCLK	VCC3_SB	SIO, ICH10, PCI EXPRESS[X16][X1]
SMBCLK_ISO	VCC3	DIMM, CLK GEN, MS7

Jumper Setting

JBAT1	(1-2)Normal	(2-3)Clear CMOS
JCI1	(1-2)Normal	(2-3)ME Disable for FPROG
J1	(1-2)short: Normal	(1-2)Open: Clear PW

LGA775-CPU		
0.8375V - 1.6000V Core	-	84A
1.1V FSB Vtt	-	4.6A

Eaglelake (GMCH)		
1.1V FSB_VTT	-	1.2 A
1.1V Core TBD (USE LB)	-	13.8A
1.1V DMI/PCI Exp.	-	2.47 A
1.5V VCC_DDR	-	3.33A
1.5V VCC_SMCLK	-	350mA
3.3V VCCA_DAC	-	66 mA
3.3V VCC33	-	15.8mA
1.1V Vcc CL	-	4.3A

ICH10		
1.1V DMI	-	41 mA
1.1V Core	-	1.16A
1.5V_A USB/SATA/PLL	-	1.652A
1.5V_B PCI Exp.	-	0.646A
VCCRTC	-	6 uA
3.3V CL	-	19 mA
1.5V GbE LAN	-	87 mA
3.3V VccSus3_3	-	200mA
3.3V Vcc3_3	-	308mA
3.3V 10/100 LAN	-	19 mA
3.3V GbE LAN	-	1 mA
3.3V HDA	-	32 mA
3.3V SusHDA	-	33 mA

HD Audio ALC262VD		
3.3V AUDIO	-	40mA
5V AUDIO	-	200mA

IDTCV184-2		
3.3V VDD_48/PCI/REF	-	250mA
0.3V-1V CPU/SRC/DOT/PLL	-	80mA

Boazman GbE		
3.3V_SB I/O & LED	-	15.5mA
1.8V AVDD	-	418.2mA
1.0V Core	-	277.2mA

ISL6334		
VCCP VRD11.1	-	0.8375V-1.6000V
3-Phase Switch	-	

W83310DS		
VTT_DDR	-	0.75V Linear 0.83A

MS11+ SW-Power		
VCC_DDR	-	1.5V PWM 13.86A

MS11+ SW-Power		
V_1P1_CORE	-	1.1V PWM 23.27A

MS7 Controller		
V_1P1_CL	-	1.1V Linear 3A

V_1P5_ICH		
1.5V Linear	-	2.385A

VCC3_SB		
3.3V Linear	-	3.96A

5VDUAL1		
5V Switch	-	4.367A
5VDIMM		
5V Switch	-	8.29A

DDRIII x2 & TERMINATOR		
0.75V VTT_DDR	-	1.2A
1.5V VCC_DDR (S0,S1)	-	3.6A
1.5V VCC_DDR (S3)	-	TBDmA

PCI Express x16 slot		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

AGP Extender riser slot		
	Luner Eagle	
+12V	-	1A
+5V	-	5.0A
+3.3Vaux	-	750mA
+3.3V	-	10.6A

PCI_E x1 slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	3.0A

PCI slot		
+12V	-	0.5A
+3.3Vaux	-	375mA
+3.3V	-	7.6A
+5V	-	5.0A

USB x 8		
+5V (S0,S1)	-	4A
+5V (S3)	-	20mA

PS2		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA

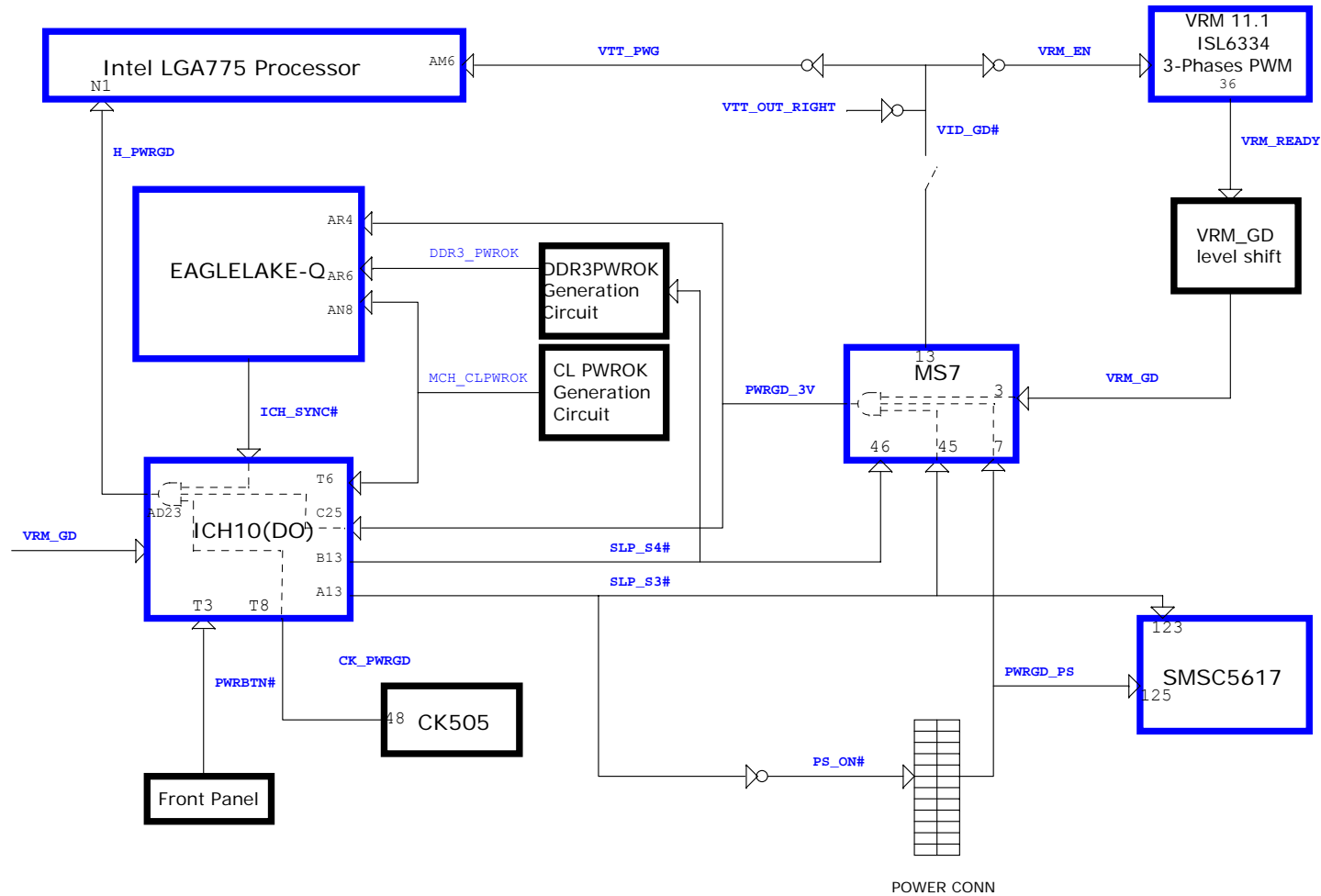
5VAudio
+5VR
500mA

+12V
ATX
2x2

+5V +3.3V +5VSB +12V
ATX POWER

3V
Battery

PWROK MAP



■MS-7420N1-970317.DSN		Notes
1Remove R414,R415.....	Have not used	
2Delete R91.....	Have not used	
3short R84 immediately.....		
4short R51 immediately.....		
5short R271 immediately.....		
6short R474 immediately.....		
7C22,C27,C474,C476 0805 to 0603.....	Unify the materials	
8R156 change to 0402.....		
9R67 change to 0805.....	Unify the materials	
10reserve C128.....	RC timing	
11Delete R246,C224,C209,C213,L14.....	Have not used	
12change C356 to 0.1u X7R.....	Follow INTEL design	
13C356,C366 change to X7R.....		
14Remove R193,C166,Q32,R285,C239,Q43;add R183,R302;Add R474,R515 between RAM_DRY and 5V_DRV_F.....	same Astoried-Z,ROPROS	
15change Q59,Q63 to dualtype.....		
16Reserve R51	Intel suggestion	
17R493,R495 change to VTT_OUT RIGHT.....	Due to layout route and follow INTEL design update	
18Empty R310,R303.....	INTEL design update	
19Add JLPC1 debug circuit.....	For debug ,MP remove	
20Change GMCH from A0 steepig to A2 steeping.....		
21Remove R333.....	GPIO18 is already output function,don't need to pull-up.	
22change COM2(SPI debug port) power source to V_3P3_CL.....	update to same the SPI ROM (U15) power source	
23Delete R357.....	Have not used	
24Delete R281,R282	Have not used	
25Remove EC29.....	V_IPI_CORE power ripple noise OK	
26Delete EC54.....	Have not used	
27Delete EC62,Add C438,EC63 stuff.....	VCC_DDR ,VTT_DDR power ripple noise OK	
28Delete INTR1.....	Have not used	
29Add C552,change CHOKE2,CHOKE7,CHOKE8 to 0.5uH,chane R90,R73,R112 to 0.09K,change C76 to 470P,R65 to 1.69K.....	For transient ,efficiency and load line	
30update U14 library,reserve R137,add C209 1uF.....		
31Remove Q40,R272.....	INTEL PS1# design update	
32Reserve Q59	Substitute Q39 circuit ,Verification when getting latest CPU	
33Add level shift between PROCHOT# and ICH10 pinK2(GPIO32).....	For NEC ENCONOMY MODE	
34Delete R94 and add D23.....	Due to PECI_REQUEST have electric leakage ,SMSC have workaround to add a diode to avoid.	
35change C145,C311,C317 to 1U 0805 X7R.....	Unify the materials	
36I20 change to 0ohm ,delete R343.....	noise OK	
37update L25,L18 description.....		
38Delete C156,C169,C178	For EMI request	
39C158,C171,C179,C161,C174,C182 change to 5.6P,Add C49C50,C51,C53	For EMI	
40Add C530 ,C436,C473 to 0.01u;Add C450 to 0.1uF.....	For EMI	
41Change Q69,Q70 to daul type,delete R488.....	Unify the materials	
42stuff R392.....	support danbury tec.	
■MS-7420N1-970317 B.DSN		
43stuff R269,R51,C345,Remove Q90.....	Use ICH10 DRAMPWROK function pin.	
44Cahnge E33,EC31,EC29 to EL cap 1800uF	for dynamic load(24A) overspec.	
45C117,C118 change to 47P.....	for crystall (accuracy),next version change to SMT type 20ppm.	
46R283,R584 change to 1.02K.....	finetune VCC_DDR,V_IPI_CORE POWER	
47EC52 change to 1800u(EL).....	for dynamic load(3A) overspec.	
48F_USB1 change to new connector.....	F_USB1 change to new connector (pin length is 4.0 mm)	
■MS-7420N1-970526.DSN		
49Add C369.....	for reducing CPU GTLREF1 ripple circuit.	
50change Q45 to A3 stepping,ICH10D0 to B0 stepping.....		
51L11,L10,L9 change to 0.1uH;C179,C171,C158 change to 8.2pF	for RGB rasing and falling time ,EMI .	
52choke6,choke5 change to 1.2uH ,15A	1.reduce layout space 2.cost a little up,but mererial is good than old choke 3.slove factory manufacture issue. 4. Unify the materials with MSI	
53CoIL2 change to 1.1uH 27A	1.reduce layout space 2.cost a little up,but mererial is good than old choke 3.slove factory manufacture issue. 4. Unify the materials with MSI	
54CoIL1 change to 05.uH 40A.....	1.get the dynamic good waveform 2.reduce layout space 3.cost a little up,but mererial is good than old choke 4.slove factory manufacture issue. 5. Unify the materials with MSI	
55R284,R283 unmount,change bace R281,R282 of MS7 ViP1_VREF circuit.....	because MS-7 inside LDO function,it has only +- 2% range than VCC3_SB +-5%	
56Remove R583,R584,Add U36,R343,R595,C606,C605.....	DDR reference voltage change to use LDO circuit.	
57Remove C36.....	C36 surplus,it has already C92.	
58reserve R243.....	for new DVI card reserve.	
59Delete C366.....	C366 is repetition with C363	
60RN4 power pin short together(pin2,4,6,8).....		
61Delete R475,R476.....	No use.	
62D23 change to 5817 diode.....	Due to 5817 has low forward voltage(0.2V) .	
63change EC23,EC24 to same EC66 component.....	Unify the materials	
64change EC58,EC68 to same EC3,EC69 component.....	Unify the materials	
65change C7,C19,C191,C256 to same C24.....	1.Unify the materials 2.due to C7,C19,C256,C191 only one source.	
66Remove J2.....	No use.	
67change C252,C490 to 0805 6.3V 10uF.....	Unify the materials	
68R351 change to 1.02K.....	design guide update.	
69Add C452.....	For EMI	
70Add C156.....	For EMI	
71change Q58,Q64,Q82,Q83 dualtype.....		
72Delete R467,R507,R494,R505.....	LE TPD is 65W,don't need to reserve it for Kentsfield CPU.	
73Delete R414,R415.....	Delete reserve thermal diode function,we use PECI.	
74Add R271,reserve R357.....	For DPRSLPVR reserve.	
■MS-7420N1-970526 A.DSN		
75Change R55 to 120 ohm.....	For LED brightness.	